Universidade de Aveiro
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Departamento de Electrónica, Telecomunicações e Informática

Pedro Miguel Duarte Cruz

Caracterização de Sistemas para Software Defined Radio

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Characterization of Systems for Software Defined Radio

Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Electrónica e Telecomunicações, realizada sob a orientação científica do Dr. Nuno Borges Carvalho, Professor Associado do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro

Dedico este trabalho aos meus pais, à minha namorada Rita e ao meu orientador Prof. Nuno Borges Carvalho, pelo incansável apoio e motivação.

O júri

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A todos o meu Muito Obrigado!

Palavras-chave

Rádio Definido por Software, Conversor Analógico-Digital, Distorção Não-Linear, Relação de Potência Pico-Média

Resumo

Esta dissertação insere-se na área de electrónica de rádio frequência, mais precisamente na caracterização de sistemas para rádios definidos por software (SDR). Um SDR é aquele que possui a flexibilidade para sintonizar, filtrar, ajustar a taxa de transmissão e controlar o tipo de modulação através de *software*. O aparecimento de novas tecnologias no mercado obriga à utilização de uma quantidade considerável de hardware nos dispositivos de transmissão/recepção, assim uma solução consiste no uso de arquitecturas de SDR onde a conversão do sinal analógico para digital é executada o mais próximo possível da antena e, sendo depois todo o processamento efectuado digitalmente. Assim, nesta tese, é apresentado um modelo comportamental para receptores de SDR, que leva em conta os elementos chave da distorção não linear. Além disso, são apresentadas algumas comparações entre simulações e medidas usando sinais multi-seno e WiMax usando um receptor ideal de SDR. Finalmente, é proposto um novo sistema de caracterização para dispositivos de SDR.

Keywords

Software-defined Radio, Analogue-to-Digital Converters, NonLinear Distortion, Peak-to-Average Power Ratio

Abstract

This dissertation is related to the radio frequency area, more specifically to the characterization of systems for software-defined radio. A software-defined radio is one that has the flexibility to tune, filter, set the transmission rate and control the modulation type only by software. The emergence of new technologies in the market forces the use of a considerable quantity of hardware in the transceivers systems, so a viable solution for this is to use SDR solutions where the analogue to digital conversion is made closest possible of the antenna and then make all the processing digitally. So, in this dissertation, a behavioral model for SDR front end receiver evaluation, that captures the key elements of the nonlinear distortion, is proposed. Moreover, some comparisons between measured and simulated results under multisine and WiMax excitations are presented using the ideal SDR receiver. Finally, a new instrumentation system for characterization of SDR front ends is proposed.

Table of Contents

List of Figures

List of Tables

List of Acronyms

1G	First Generation
2G	Second Generation
3G	Third Generation
4G	Fourth Generation
ACPR	Adjacent Channel Power Ratio
ADC	Analogue-to-Digital Converter
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone System
AWG	Arbitrary Waveform Generator
BER	Bit-Error-Rate
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CCDF	Complementary Cumulative Distribution Function
CDF	Cumulative Distribution Function
DAC	Digital-to-Analog Converter
DFT	Discrete Fourier Transform
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
DUT	Device Under Test
EDGE	Enhanced Data rates for GSM Evolution
EVM	Error Vector Magnitude
FDD	Frequency Division Duplex
FET	Field-Effect Transistor
FM	Frequency Modulated
FPBW	Full Power Bandwidth
GPIB	General Purpose Interface Bus
GPRS	General Packet Radio Service

GSM	Global Systems for Mobile Communications
HF	High Frequency
IC	Integrated Circuit
ICNIA	Integrated Communications Navigation and Identification Avionics
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate-Frequency
IMD	Intermodulation Distortion
INL	Integral Nonlinearity
IS-95	Interim Standard 95
JTRS	Joint Tactical Radio System
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
LTE	Long Term Evolution
MIT	Massachusetts Institute of Technology
MMITS	Modular Multifunction Information Transfer System
MTA	Microwave Transition Analyzer
MTT-S	Microwave Theory and Techniques Society
NPR	Noise Power Ratio
OFDM	Orthogonal Frequency Division Multiplexing
PAPR	Peak-to-Average Power Ratio
PDF	Probability Density Function
PRBS	Pseudo-Random Binary Sequence
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAR	Successive Approximations shift Register
SCA	Software Communications Architecture
SDR	Software-Defined Radio

SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
UHF	Ultra High Frequency
UMTS	Universal Mobile Telecommunications System
USRP	Universal Software Radio Peripheral
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio
WiMax	Worldwide Interoperability for Microwave Access

Chapter 1

Introduction

In the end of the 19th century, *James Clark Maxwell* predicted the existence of radio waves and later *Heinrich Rudolph Hertz* demonstrated that rapid variations of electric current could be projected into the space in the form of radio waves. After that, there was been an unprecedented set of discoveries and a varying disputed claiming about who invented the radio, which in the beginning was called “wireless telegraphy”. This invention is normally attributed to *Guglielmo Marconi* with a patent attribution [1] "*for improvements in apparatus for wireless telegraphy*", but *Nikola Tesla* early also have demonstrated the wireless telegraphy attested with two patents [2-3]. Many other scientists have contributed to the development of radio transmissions. This was a remarkable point in the history of radio that has given the first step to the revolution in circuits, technologies and theories related to the radio transmission, that still tough in our time.

Since there the constant evolution of the wireless communications systems happens, starting with the Amplitude-Modulated (AM) broadcast radios and a bit later with the Frequency-Modulated (FM) broadcast radios that have improved the quality of radio transmissions. However, the truly newcomer to the wireless world was the cell phone technology. This one started with the Advanced Mobile Phone System (AMPS) technology in 1980’s and was recognized as first generation (1G) communication.

The next phase was the second generation (2G) which brought digital technology for voice communication to the mobile phone system approximately in 1990 and continues to be used today. The most known standards belonging to this generation are the Global System for Mobile Communications (GSM) [4] used in Europe and Interim Standard 95

(IS-95) used in United States of America. The reduced costs, the full mobility and high voice quality service allowed 2G systems to have a penetration tax above one hundred per cent which turned it into one of the biggest commercial success ever.

Although, to meet the growing demands in network capacity, rates required for high speed data transfer and multimedia applications, 3G standards started evolving, being this systems essentially a linear enhancement of 2G systems [5]. Currently, transition is happening from 2G to 3G systems, where several new standards were proposed like EDGE (Enhanced Data rates for GSM Evolution), GPRS (General Packet Radio Services), UMTS (Universal Mobile Telecommunications System), WiMax (Worldwide Interoperability for Microwave Access), etc.

Further, the constant appearance of new standards has caused emerge of a new generation, the 4th generation (4G). This one is being developed to accommodate the quality of service (QoS) and allowing the interoperability between the existing wireless standards [6-7]. Since 4G is a collection of wireless standards, the final form of 4G device will constitute various standards, and this can be efficiently realized using Software-defined Radio (SDR) technology as explained in next section. Next figure presents the evolution of the several generations of wireless communications and appoints the market chance for SDR solutions.

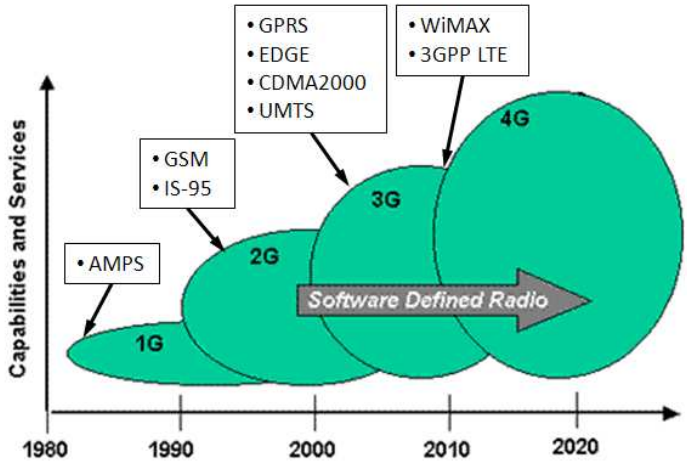


Fig. 1 - The market opportunity for SDR technology, extracted from [8]

1.1 Motivation

With the constant evolution of new technologies standards (GSM, IEEE 802.11a/b/g/n, UMTS, WiMax, etc) the wireless communication industry is facing new challenges, either the difficulty of integration of these standards or the incompatibility between them in the different countries. So, this scenario inhibits the deployment of a global roaming network.

One important enhancement in this field is the SDR technology [9] that has the ability to solve most of these problems. Since, with the use of multiple modules implementing different standards, the system can take up different personalities depending on the module being used. In other words, the same piece of hardware (called RF front end) can perform different functions at different times, further the reconfiguration of the terminal can be made by executing a new software module from their own memory card or through a downloadable module over the air.

Moreover, the reconfiguration of SDR devices will greatly facilitate the roaming from region to region where different commercial wireless standards are deployed or even within a given country in which different air interfaces are utilized. These reconfiguration data can be new modulation techniques, new power levels, new operational frequencies or the use of a new technology standard.

So, the possibility of reconfigure the terminal only by executing a new software module is much easier and cost advantage than physical recall of the devices or the use of a new hardware module. As well as transmitting information, SDR may have value in the emerging field of localization systems (using radio frequency techniques) where devices operating on various frequencies and using various communication protocols can improve the precision and accuracy of these systems [10].

1.2 Dissertation Overview

This dissertation is organized into the following sections, in **Chapter 1** an introduction about the communications evolution is made from their beginning and the motivation for this work is provided. **Chapter 2** presents a brief overview about the Software-defined Radio history and several receiver front end architectures. Also, describes architectures and

main characteristics of Analog-to-Digital Converters. Next, in **Chapter 3** some concepts related to signal information, bandpass sampling and peak-to-average power ratio are presented. Furthermore, the nonlinear distortion causes in SDR receivers are analyzed in detail. In **Chapter 4**, to confirm the statements that are presented in previous chapter, a behavioral model for SDR front end receiver is proposed accounting with all of the nonlinear distortion causes. Then, some comparisons between measured and simulated results are shown. Further, **Chapter 5** shows a new instrumentation system for characterizing the Software-defined Radio receiver front ends based on simple laboratory equipment. Finally, **Chapter 6** presents some conclusions and suggestions for future work.

During the elaboration of this dissertation the following original contributions were made:

[1] Pedro Cruz and Nuno B. Carvalho, "PAPR Evaluation in Multi-Mode SDR Transceivers", *European Microwave Conference Dig.*, Amsterdam, Netherlands, *pp. tbd*, October 2008.

[2] Pedro Cruz, Nuno B. Carvalho, Kate A. Remley and Kevin G. Gard, "Mixed Analog-Digital Instrumentation for Software Defined Radio Characterization", *IEEE MTT-S Int. Microwave Symp. Dig.*, Atlanta, Georgia, United States, *pp. tbd*, June 2008.

[3] Pedro Cruz, Nuno B. Carvalho and Kate A. Remley, "Evaluation of Nonlinear Distortion in ADCs Using Multisines", *IEEE MTT-S Int. Microwave Symp. Dig.*, Atlanta, Georgia, United States, *pp. tbd*, June 2008.

Chapter 2

State of the Art

In this chapter several background concepts about Software-defined Radio (SDR) and about one of its most important components (the Analog-to-Digital Converter, ADC) are introduced.

2.1 Software Defined Radio

The concept of SDR first appeared with the work of J. Mitola [9] in 1995. In this work, he purposed to create a radio that is fully adaptable by software, enabling the radio to adapt to several communication scenarios automatically.

Mr. Mitola is quoted as saying, "*A software radio is a radio whose channel modulation waveforms are defined in software. That is, waveforms are generated as sampled digital signals, converted from digital to analog via a wideband DAC and then possibly upconverted from IF to RF. The receiver, similarly, employs a wideband ADC that captures all of the channels of the software radio node. The receiver then extracts, downconverts and demodulates the channel waveform using software on a general purpose processor.*" This concept is illustrated in Fig. 2.

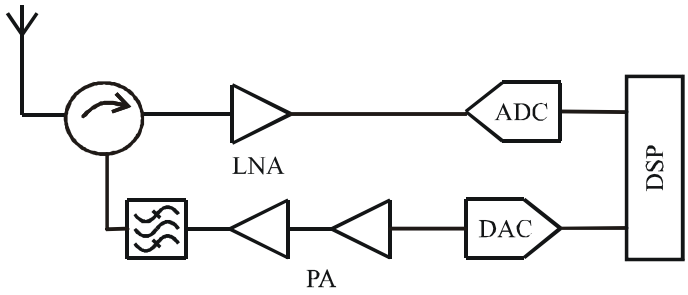


Fig. 2 - Ideal SDR Concept

The ideal SDR will adapt to the transmission scenario by gathering information about all of the signals that are present in the air interface. This necessitates use of a system that can scan the spectrum from low to high frequencies by software means. This concept has driven many researchers to study cognitive radio approaches [11], where the radio adapts itself to the air interface by optimizing the carrier frequency, modulation and choice of radio standard to minimize interference and maintain communication in a given scenario.

In the following, a brief review of the history of SDRs and an explanation of the possible SDR receiver front end architectures are presented.

2.1.1 History of SDRs

In the 1970's, the U.S. Air Force and U.S. Navy in order to meet the growing needs for communications, navigation and identification, decided to initiate the Integrated Communications Navigation and Identification Avionics (ICNIA) program [12]. This was one of the first systems to use DSP-based programmable modem and control to obtain a fully integrated capability for airborne platforms. Prior technology required a set of independent federated hardware modules.

The ICNIA architecture was split into receive and transmit paths interconnected with data paths, control and spread spectrum busses. Also, this uses a reprogrammable digital signal processor (DSP) to operate multi-function multi-band airborne radios in the band from 30 to 1600MHz, Fig. 3. The ICNIA technology provided the foundation for many military-radio programs.

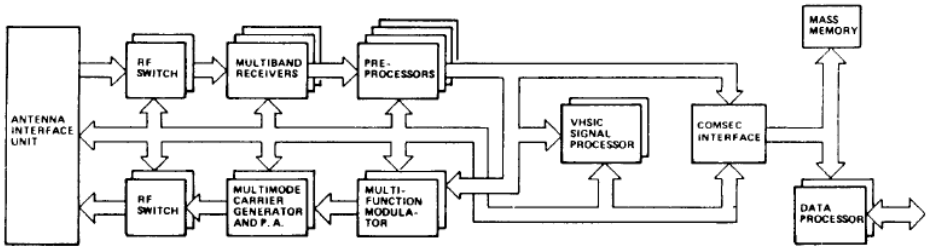


Fig. 3 - Architecture of ICNIA system, extracted from [12]

Later, a new military program come out based on ICNIA technology and was called SPEAKeasy [13-14]. This is a two phase's program, the first one had started on 1992 until 1995 and the second one from mid of 1995 to 1999.

The SPEAKeasy had two main objectives, to develop a modular and reprogrammable modem with an open architecture and to develop a generic software architecture to facilitate the addition of new waveforms.

The phase-I program was to demonstrate a four-channel, wideband architecture for high-speed frequency-hopped and pseudorandom spread-spectrum waveforms. It had to operate over the military HF, VHF and UHF frequency bands. However, RF studies established that the operating range from 2MHz to 2GHz had to be divided in three different bands. The low band ranged from 2 to 30MHz, the middle band ranged from 30 to 400MHz and the high band ranged from 400MHz to 2GHz. The phase-I equipment was demonstrated on the air in June 1995 but only for the middle band RF section.

The design goals of phase-II were to upgrade the solution presented in phase-I in order to make them smaller, weigh less, cheaper and to develop the remaining RF sections in order to complete the entire proposed band from 2MHz to 2GHz. The phase-II was to be a four-year research and development program but, in March 1997, with only 15 months into the program a demonstration radio was produced for the middle band range from 30 to 400MHz.

Due to the success of SPEAKeasy program, particularly in phase-II, a decision was made to immediately enter production rather than invest in further research and development. Consequently, phase-II had no opportunity to implement the full RF range.

In early 1998 another government program, the Joint Tactical Radio System (JTRS) [15], uses SPEAKeasy technology in a family of interoperable, multi-band, networked SDRs. The JTRS program provides a flexible new approach to meet diverse warfighter

communications needs through software programmable radio technology. All functionality and expandability is built upon the Software Communications Architecture (SCA). Thus, by developing and implementing an open architecture of cutting-edge radio waveform technology multiple radio types (e.g. handheld, ground-mobile, airborne, maritime, etc.) can communicate with each other. The ultimate goal is to produce a family of interoperable and modular SDRs that operate as nodes in a network to ensure secure wireless communication and networking services for mobile and fixed forces. These goals extend to U.S. allies, joint and coalition partners.

These concerns are not unique to the military and have resulted, around 1996, in the creation of Modular Multifunction Information Transfer Section (MMITS) Forum that later was called SDR Forum [16]. It was created to facilitate the adoption of radio standards for software-defined radio systems with open system architecture. Such systems are required by military communications and commercial service providers [17].

Next figure presents the evolution of military SDR solutions, until these days.

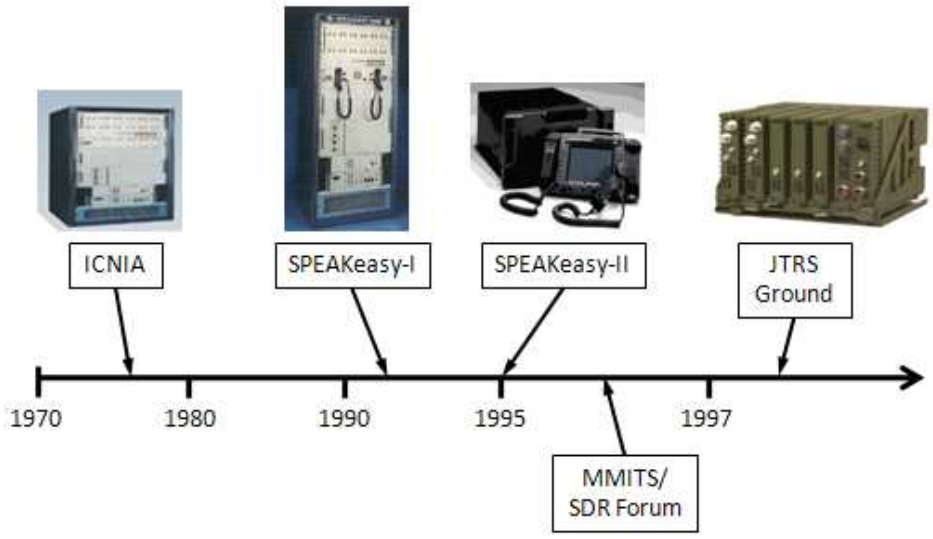


Fig. 4 - Timeline of military SDR solutions

Since there, SDR research is being pursued not only in industry but also in academia. For example, two SDR research programs in academia were carried on at the Georgia Institute of Technology [18] and at the Massachusetts Institute of Technology (MIT) [19]. For instance, the SDR of Georgia Institute of Technology has the capability to demodulating OFDM, BPSK, QPSK and QAM signals. On other hand, the prototype of

MIT known as Handy 21 is based on a handheld computer that combines the functions of cellular phone, wireless connection, pager, AM/FM radio and television set.

Also, in the commercial panel several solutions are available, going from the amateur FLEX-5000 family from FlexRadio Systems [20] to the well known open-source SDR platform from GNU Radio that uses the Universal Software Radio Peripheral (USRP) from Ettus Research LLC [21], which is presented in Fig. 5.

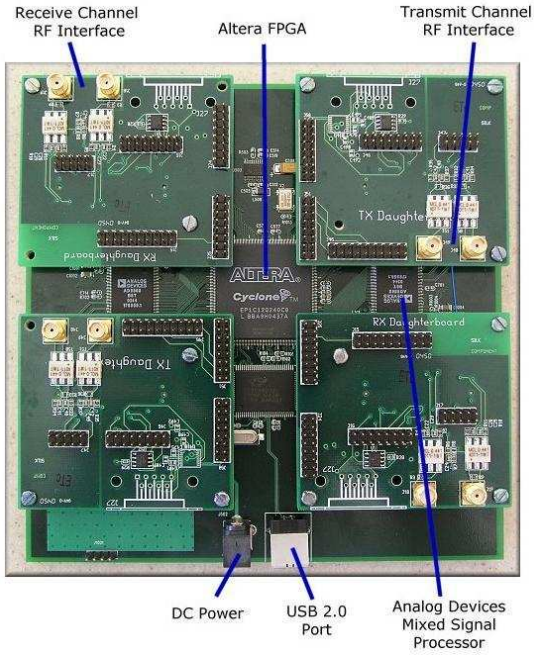


Fig. 5 - Motherboard and daughterboard's of USRP family, extracted from [21]

2.1.2 Front End Receiver Architectures

In this section, several RF front end architectures that can be potential appliance to the SDR receivers are succinctly reviewed. Depending on the location of the ADC in the receiver chain, the basic receiver architectures can be split into three categories [22].

In the first category, Fig. 6, the ADC is placed at baseband. The signal traverses two down conversion stages with filtering and is amplified at RF by an LNA; the purpose is to shift the desired signal to the baseband. Such architecture is currently adopted in most radio receivers. The advantages of this receiver architecture derive from the availability of low cost narrowband RF and IF components with low power consumption. However, due to its narrowband intend, it has the drawback that the design of main components is made to a specific channel and is hard to expand the receiving band.

So, for a SDR approach this architecture is not a good alternative because of its narrow and fixed band design and the fact that the integration in a single Integrated Circuit (IC) chip is difficult because the number of discrete components required.

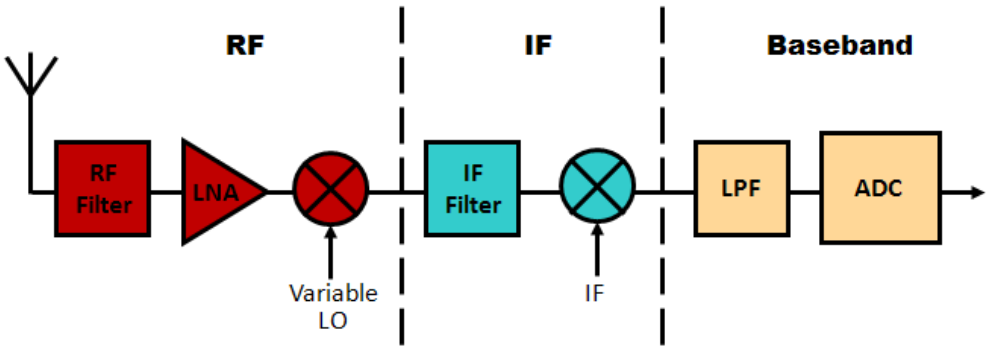


Fig. 6 - Simple super-heterodyne front end architecture

The second category considers the ADC in the IF section, preceded by a RF filter (that eliminates out-of-band interferes), a LNA and a mixing stage, Fig. 7. The down conversion stage is identical to the first stage used in previous implementation. Compared to the previous architecture, this could be designed to operate over a wider bandwidth because following the down conversion the entire bandwidth can be filtered and digitized allowing digitally processing of that. Thus, one advantage is the possibility of receive more than one channel and then isolate each one using digital filtering.

This architecture is an approximation of the ideal SDR receiver configuration that will be explained next. Moreover, this architecture is realizable with actual available components.

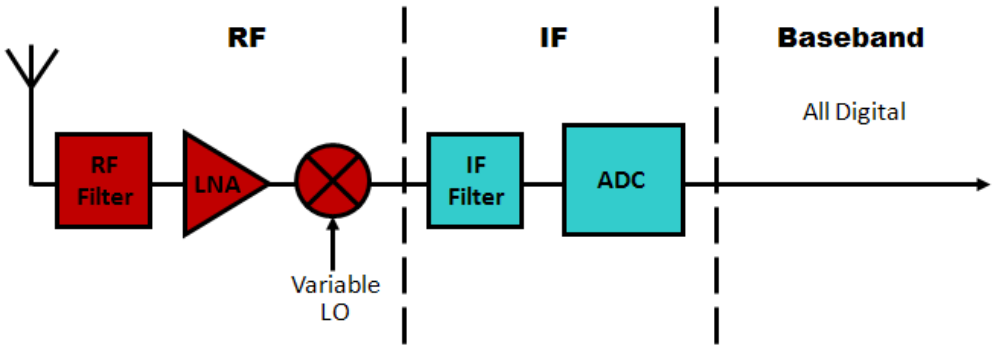


Fig. 7 - Single down conversion front end architecture

Finally, the third category, Fig. 8, digitizes the signal at RF. This architecture corresponds to that envisioned by Mitola and is the most challenging for future approaches and the most appropriate for multi-standard operation. Unfortunately, this architecture is not practical because for that the ADC must fulfill extraordinary specifications; either a very high sampling rate to digitize a minimum frequency band in the order of tens of GHz or the high dynamic range that will be required. Furthermore, other limits exist as the mandatory ADC linearity over the entire frequency range and the power dissipation of such devices that would prevent their use in mobile applications.

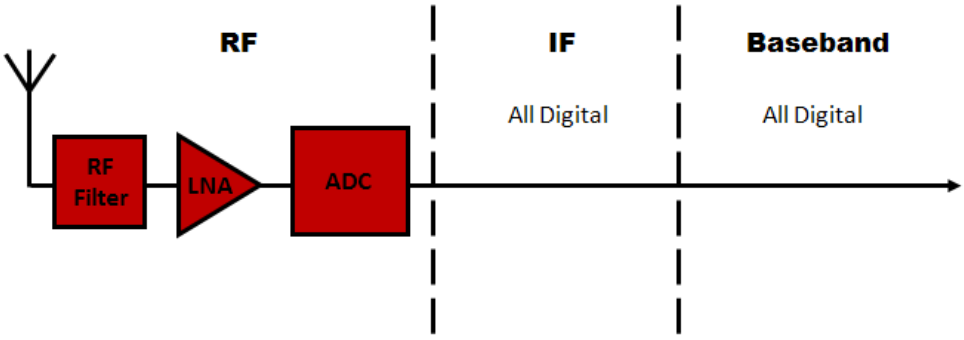


Fig. 8 - Direct digitization front end architecture

2.2 Analogue-to-Digital Converters

The Analog-to-Digital Converters (ADC) are becoming an electronic sub-system key component in recent Software-defined Radio (SDR) front end receivers [9], see Fig. 2.

The recent advances of ADC sub-systems, allows the higher frequency bands to be digitally converted to the digital domain immediately, without the need for any further down-conversion, and thus obtain all the digital domain advantages that arise from that fact. The ADC world has been evolving very fast, as can be seen from Fig. 9, a state of art graph with the architecture and application scenarios of most of the ADC architectures (see chapter 2.2.2). Commercially available ADCs are now operating at frequencies in the order of gigahertz [23] enabling the ideal SDR concept.

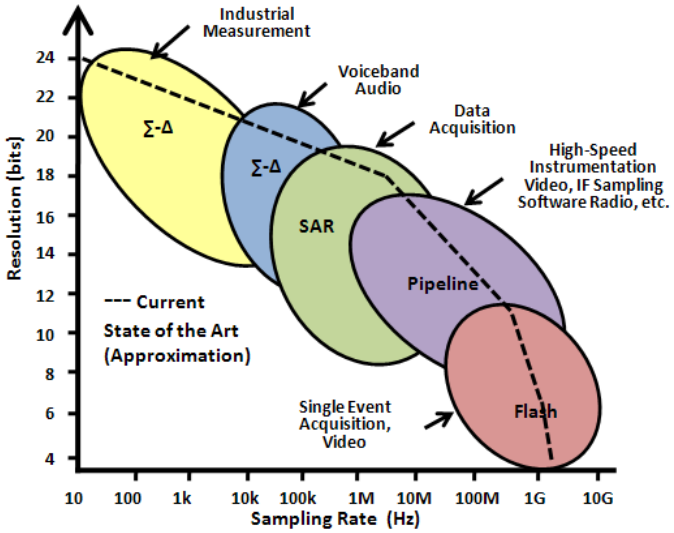


Fig. 9 - ADC evolution map, extracted from [24]

Nevertheless the approach for characterizing ADC's as been normally devoted to low frequency and static approximations of the ADC itself.

There are two main standards that are related to ADC characterization, the IEEE Std 1241-2000 [25] and the IEEE Std 1057-1994 [26], these two standards combined and specially the first one, that is related exclusively to ADC's, state the main important characteristics of the ADC measurement in nowadays ADC state of art.

2.2.1 ADC Basics

For a radio engineer and analog system researcher, the first way to start on ADC's is by looking at its typical configuration, Fig. 10. There two fundamental blocks can be seen, the sample and hold and the quantizer. Actually these are the two fundamental blocks that allow a correct conversion from analog to digital domain.

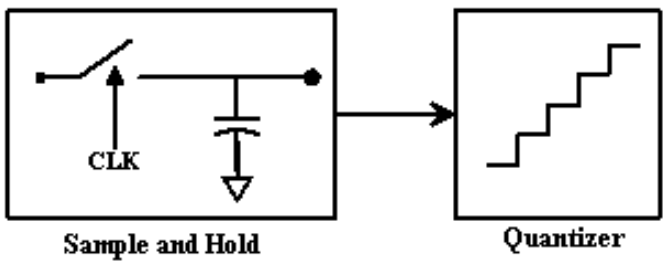


Fig. 10 - Ideal sample and hold followed by an ideal quantizer

Since the ADC needs a certain amount of time to convert from the analog continuous domain to the digital world (bit) domain, then the voltage should be maintained at a constant value, so it can be quantized and then converted into bits.

This sample and hold, should obey the entire signal processing rules about sampling rate, Nyquist frequencies and so on, in order not to disrupt the signal it is being analyzed. A sampler transforms an analog signal, $x(t)$, into its sampled equivalent, $x[n]$. For uniform sampling with period T the input signal is given by:

$$x[n] \equiv x(nT) = \sum_{n=-\infty}^{+\infty} x(t).\delta(t - nT) \tag{1}$$

In Fig. 11 the signal before and after the sample and hold can be seen and it is obvious there is already some form of quantization of the signal in this block. But this quantization can be called linear that is actually retaining the input signal. Whenever, it is only for a certain amount of time, normally the time needed for the conversion.

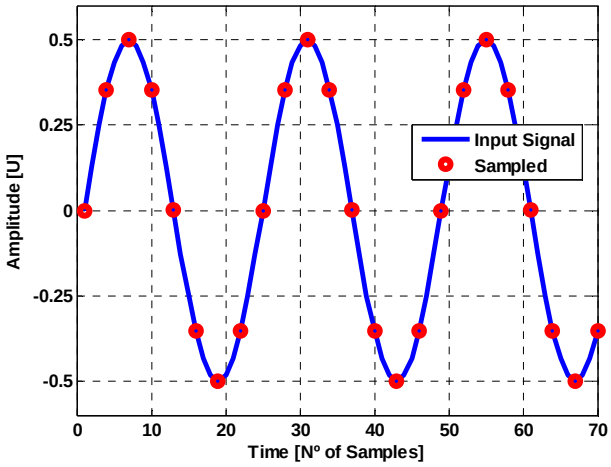


Fig. 11 - Figure of input analog signal and sampled signal

In the next block the digital quantization is implemented, by quantization can be defined as the process of approximating a continuous range of values (or a very large set of possible discrete values) by a relatively-small set of discrete values. Assuming that $V_{Full\text{-}Scale}$ is the range of the quantizer and $2^{N^{o}\ Bits}$ is the number of quantization intervals, the amplitude of each quantization interval termed by Least Significant Bit (LSB) is given by:

$$LSB = \frac{V_{Full-Scale}}{2^{N^{o}Bits}} \tag{2}$$

In fact, this is the digitization of the signal in discrete amplitudes and time values. Fig. 12 presents this effect for an ideal 3-bit ADC.

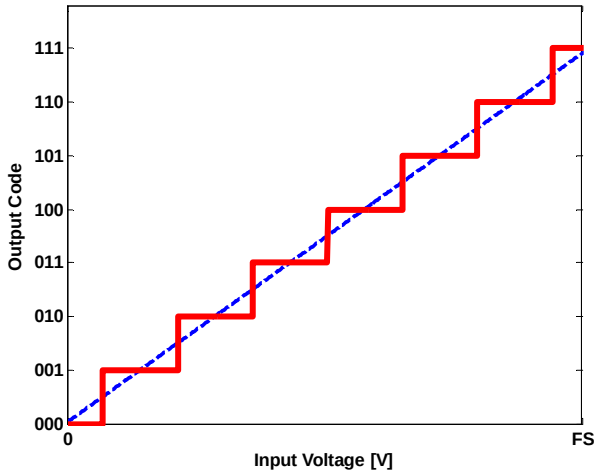


Fig. 12 - Discrete quantization of an ideal 3-bit ADC

As could be seen the quantization process is a strong nonlinear process, since imposes a radical change in the input continuous signal causing an error that is known as quantization noise. As was been stated by Bennett in [27] the maximum error of an ideal converter when quantizing a signal is ±(LSB/2). So, the quantization error can be accurate modelled using a simple sawtooth waveform and after some simplifies the *rms* quantization error can be represented by:

$$Quantization\ Noise\ rms = \frac{Q}{\sqrt{12}} \tag{3}$$

where, Q is equivalent to the LSB. Assuming a full-scale input sine-wave the theoretical SNR can be calculated using the next equation.

$$SNR = 20 * \log_{10}\left(\frac{rms\ value\ of\ FS\ input}{rms\ value\ of\ quantization\ noise}\right) \tag{4}$$

The rms value of the input signal is therefore:

$$rms\ value\ of\ FS\ input = \frac{Q.2^{N^{o}Bits}}{2.\sqrt{2}} \tag{5}$$

Other consideration that has to be accounted is the Peak-to-Average Power of the signal that is been measured. Thus, the ideal SNR value of an ideal N-bit converter is given by:

$$SNR_{dB} = 20 * \log_{10}\left(\frac{Q.2^{N} / 2.\sqrt{2}}{Q / \sqrt{12}}\right) \tag{6}$$

That can be simplified to obtain (7), where can be seen that the SNR only depends on the number of bits of converter (*N*):

$$SNR_{dB} = 6.02 * N + 1.76 \tag{7}$$

Taking in account that the actual digital modulations have high peak-to-average power signals a parameter α (Peak-to-Average Power Ratio value, explained in chapter 3.3) must be included in equation (7). This one is placed here in order to avoid the clipping of the ADC and then generate distortion.

Moreover, in several applications the signal of interest occupies less bandwidth than the used Nyquist bandwidth (f_s/2). So, if digital filtering is used to eliminate noise components outside of a determined bandwidth (BW) then, another factor (called process gain) must be included in the previous equation. Therefore, the final equation is:

$$SNR_{dB} = 6.02 * N + 1.76 - \alpha + 10 * \log_{10}\left(\frac{f_s}{2 \times BW}\right) \tag{8}$$

This process gain is normally referred as oversampling. Moreover, it is important to emphasize that the *rms* quantization is measured over the full Nyquist bandwidth, DC to (f_s/2).

2.2.2 ADC Architectures

An overwhelming variety of ADCs exist on the market today [28, 29, 30], with differing resolutions, bandwidths, accuracies, architectures, packaging and power requirements.

The most popular ADC architectures available today are flash (all decisions made simultaneously), successive approximations (also called SAR because a successive-approximations shift register is the key element), pipelined (with multiple flash stages) and sigma-delta (a charge-balancing type), [31].

Next sections show a brief review for each one of these architectures.

2.2.2.1 Flash ADC

The flash architecture [32] is a popular approach for designing very high-speed low-to-medium resolution (6 to 8 bits) converters. Fig. 13 illustrates this architecture.

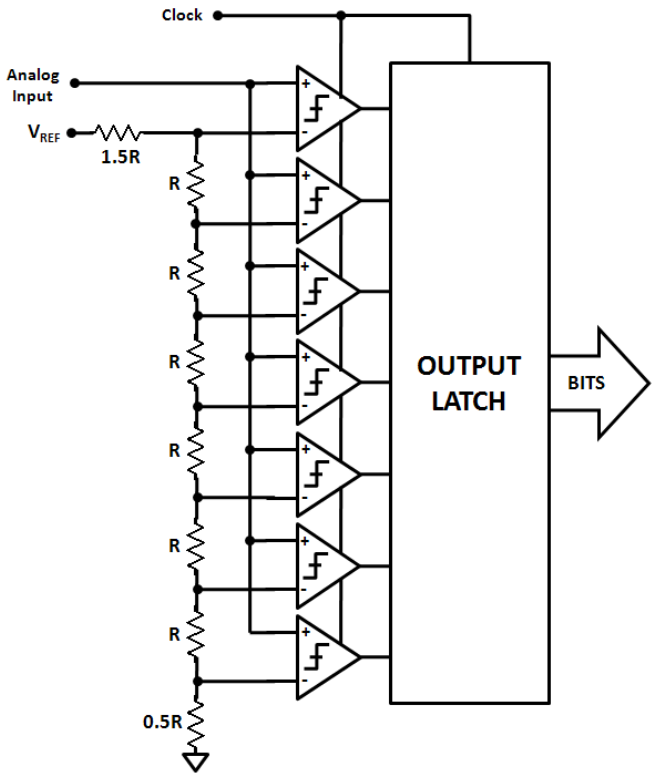


Fig. 13 – Architecture of a 3-bit flash ADC

The input signal is fed to (2^N-1), where N is the number of bits, comparators connected in parallel and is compared to a set of reference voltages generated from a resistor string and then, the output code (also called thermometer code) is then transformed to the N-bit binary code. This type of ADC is very fast due to its simple architecture, where only exists the comparator and the encoder delays. But it has several serious drawbacks as the number of comparators used. The chip area and the power consumption increase exponentially with the number of bits (N) required.

Moreover, the large number of comparators connected to the input signal also results in a large parasitic load and the accuracy requirement of the comparators also increases exponentially with N.

2.2.2.2 Successive-Approximations ADC

The successive-approximations architecture [33] can be thought of as being orthogonal to the flash architecture because, conceptually, that one uses a single comparator over many cycles to make its conversion, Fig. 14.

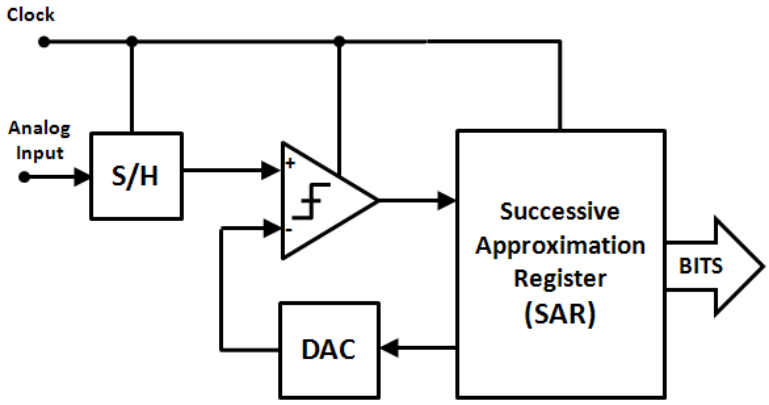


Fig. 14 – Architecture of a SAR ADC

This type of converter works as a balance scale, on one side of the scale the sampled analog value is placed and on the other side a weight is placed (generated by the SAR and a DAC) that has the value of ½ of full-scale and compare the two values. If the unknown value is larger, the ½-scale weight is retained; if the unknown value is smaller, it is rejected. This series of steps is repeated n times using successively smaller weights in binary progression (1/4, 1/8, 1/16, …, $1/2^N$ of full scale) until the desired resolution is attained.

A SAR converter can use a single comparator to realize a high resolution ADC but it requires N (number of bits) comparison cycles to achieve the N-bit resolution. For this reason, SAR converters are more often used at lower speeds in higher resolution applications and also well suited for applications that have non-periodic inputs because the conversions can be started at single moment.

2.2.2.3 Pipelined ADC

A pipeline converter [34, 35] is a generalized *p*-stage's flash ADC with improved throughput and tolerance to comparator errors. It has a sample-and-hold and an amplifier in

each stage, which allows each stage to be immediately used in the next input sample. Fig. 15 shows typical pipeline ADC architecture.

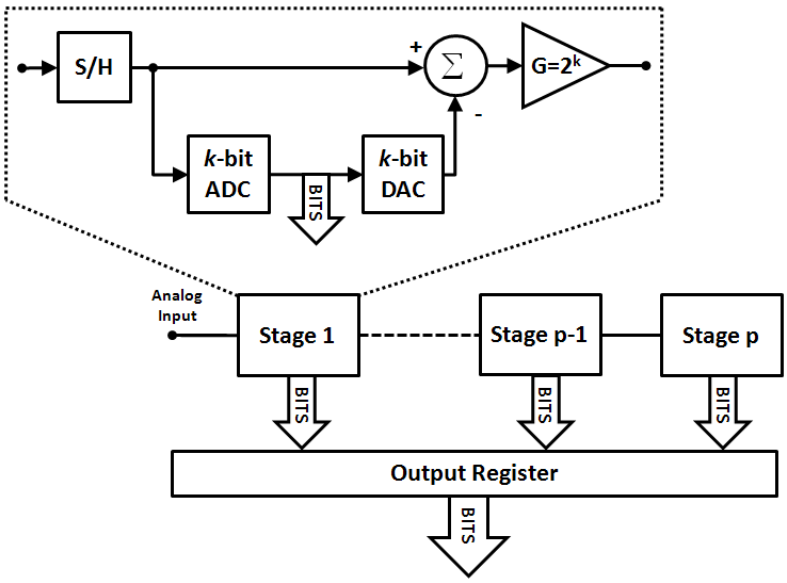


Fig. 15 – Architecture of a pipeline ADC

It consists of p identical stages, each one samples the output from the previous and quantizes to k bits digital code, which is then converted back to an analog signal by the k-bit DAC. The difference between the sample signal and the restored analog signal is amplified by a amplifier with gain of $G = 2^k$ and then passed to the next stage. Finally, the (p*k)-bit output is combined in the output register producing a high-speed ADC with a resolution of N = (p*k) bits.

The limitations of this architecture are that converter has latency equal to p (number of stages) cycles and the conversion process generally requires a clock with a fixed period.

However, due to its architecture, the throughput rate is independent of the number of stages used and the hardware cost is approximately linear with the resolution. Another advantage is that the accuracy requirements for the latter stages are greatly relaxed compared to the first stages, making it possible to reduce the total power consumption.

Based on the above reasons, pipeline ADC is the most suitable choice for broadband communications systems and Software-defined Radio receivers.

2.2.2.4 Sigma-Delta ADC

The sigma-delta architecture [36] takes a fundamentally different approach than those outlined above. Conceptually, this consists of an integrator, a comparator and a single-bit DAC (see Fig. 16). The output of the DAC is subtracted from the input signal and the result is then integrated and converted to a single-bit digital output by the comparator. Finally, the bit becomes the input to the DAC and the DAC's output is again subtracted from the input signal, etc. this closed-loop process is carried out at a high "oversampled" rate, so the digital data coming from the ADC is a stream of "ones" and "zeros". Finally, that bit stream data is digitally filtered and decimated to result in a binary-format output.

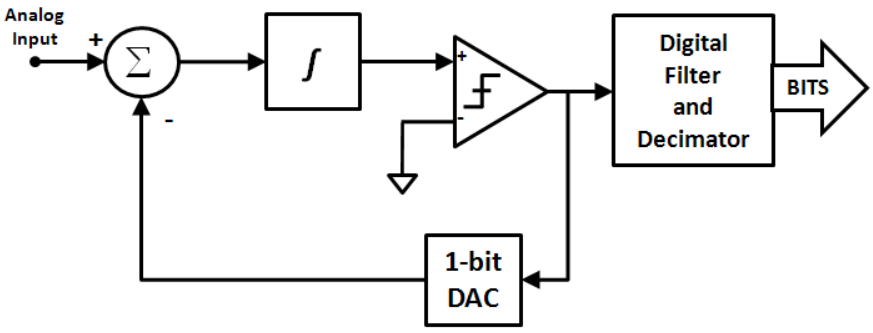


Fig. 16 – Architecture of sigma-delta ADC

A limitation of this architecture is its latency because the high oversample rate. But, one of the advantages of this type of ADC is the capability of noise shaping, which is a phenomenon where the low-frequency noise is pushed up to higher frequencies and then can be eliminated by a digital filter, Fig. 17.

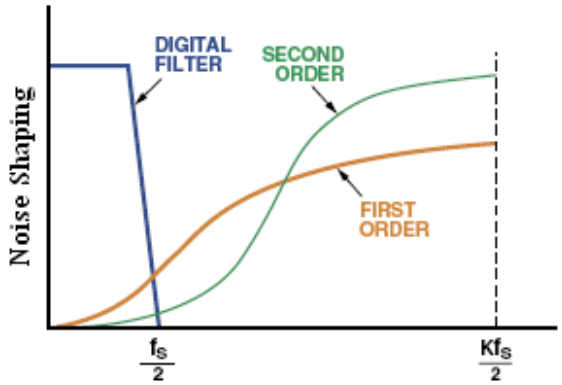


Fig. 17 - Noise shaping capability, extracted from [24]

2.2.3 Factors of Merit for Nonlinear Distortion

The nonlinear analysis of an ADC is very important to be studied and analysed, since it will impose the maximum value of signal-to-noise ratio (SNR) and thus of sensibility that we can have in a wireless receiver [37] and will also impose the maximum achievable linearization values that will be possible to obtain in digital linearizers [37, 38].

The most prominent standard in ADC testing and measurement today is described in [25]. There several testing figures of merit are described spanning, from typical static, analog, digital and noise measurements, as well as more complex characteristics, as nonlinear behaviour or dynamic evaluations.

For instance, Fig. 18 presents some of the most well known linear errors that can appear in a non-ideal ADC.

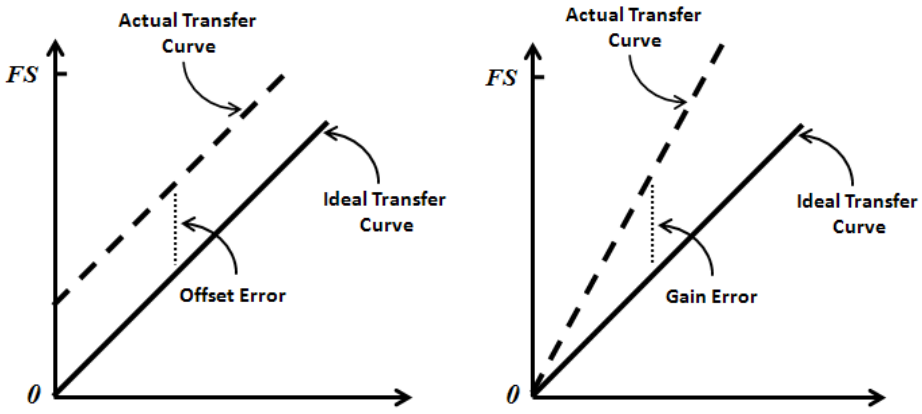


Fig. 18 - Offset and Gain Error

In this section the nonlinear behavior of the ADC's is explained succinctly. More detailed of these characteristics and others also important can be analysed in [25]. Referring to the nonlinear behavior the following figures of merit can be stated:

Differential Nonlinearity (DNL) is the difference between a specified code bin width and the average code bin width (the same of Least Significant Bit, LSB), divided by the average code bin width (LSB).

By giving a close look to Fig. 19, can be seen that differential nonlinearity can arise from many influences, either non-monotonic transfer curve of ADC, i.e., the ADC has output codes that do not increase for a uniformly increasing of the input signal or a

nonlinear transfer curve evolution. This fact can also impose missing codes that are normally due to the non-monotonic evolution of the ADC transfer curve.

Actually, the DNL can be calculated as:

$$DNL[k] = \frac{W[k] - Q}{Q} \tag{9}$$

where, W[k] is the width of code bin k, T[k+1]-T[k], Q is the ideal code bin width.

Neither the width of the top bin, W[2^N-1], nor that of the bottom bin, W[0], are defined. A code k is defined to be a missing code if DNL[k] ≤ -0.9. On other hand, perfect DNL coincides with DNL = 0.

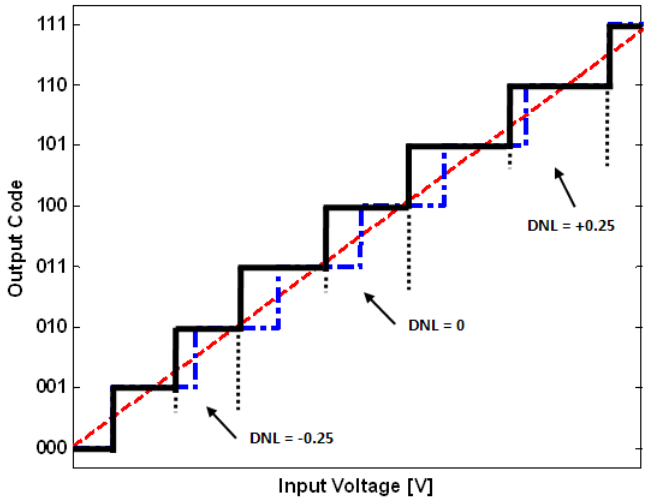


Fig. 19 - Nonlinear quantization curve with DNL values presented

From last figure it is possible to have a closer look at the ADC conversion with a severely nonlinear transfer function, with the some DNL values described.

Fig. 20 presents several types of degradations in the transfer curve that contribute significantly to the increase of total DNL, either non-monotonicity of the transfer curve or missing codes.

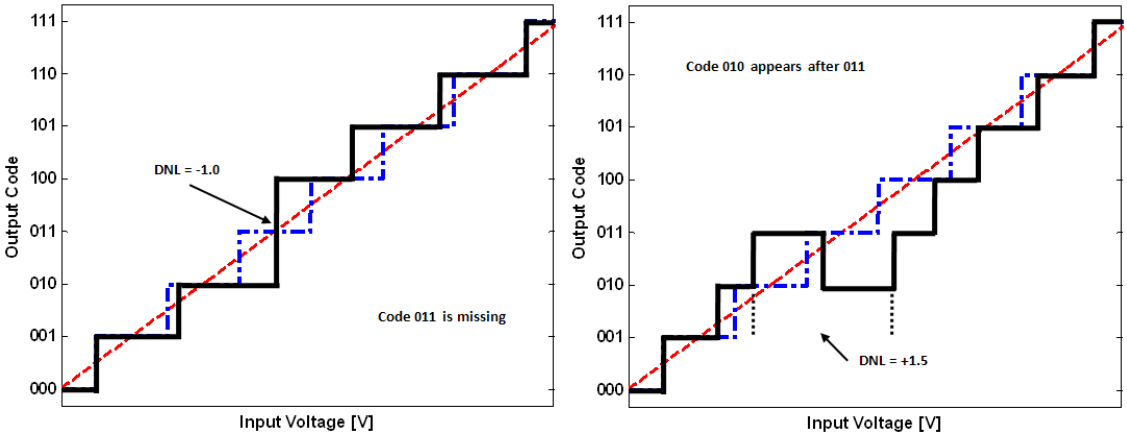


Fig. 20 - Nonlinear quantization curves with missing codes (a) and non-monotonic curve (b)

Another important measure in ADC's is their hysteresis, which impose a different transfer curve accordingly to the direction by which it is traversed. To obtain this value the ADC transfer curve should be obtained by a increasing and a decreasing input signal.

Integral Nonlinearity (INL) is the maximum difference between the ideal and actual code transition levels after correcting for gain and offset. This figure of merit actually accounts for a similar value of nonlinearity has in amplifiers that is it evaluates the maximum difference between the ideal linear transfer curve and the real nonlinear evolution. Fig. 21 presents the representation of the INL in a nonlinear ADC transfer curve.

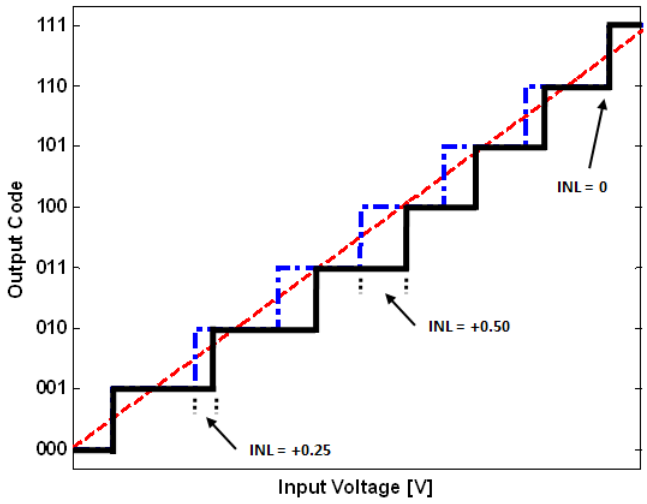


Fig. 21 - Nonlinear quantization curve with INL values presented

According to [25], the INL is measured as a function of *k* and is given in percentage by equation (10):

$$INL[k] = 100\% \times \frac{\varepsilon[k]}{2^N \times Q} = 100\% \times \frac{\varepsilon[k]}{V_{FS}} \tag{10}$$

where, INL[*k*] is the integral nonlinearity at output code *k*, *ε[k]* is the difference between T[*k*] and the ideal value of T[*k*] computed from *G* (gain error) and V_{os} (offset value), *Q* is the ideal code bin width expressed in input units and V_{FS} is the full-scale range of the ADC in input units.

This method of analysing the INL is useful only if the transitions are well defined, if not, another useful method is by measuring the transfer curve of the ADC, using the end point method or the best straight line method as described in [25]. And then compare it with a linear transfer ideal curve.

Harmonic Distortion, for a pure sine wave input, are the output components at frequencies that are an integer multiple of the applied sine wave frequency which are induced by the input sine wave. The measurement of these quantities is made by inputting a simple sine wave at the input of the ADC, and then measures each harmonic at the output.

Noise Power Ratio (NPR) is the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the discrete Fourier transform spectrum of the ADC output sample set. In [39] some more information can be obtained on how to measure this factor of merit in amplifiers. Nevertheless, a great care should be taken when doing these measurements in the ADC domain since here were normally used DFT's to measure the frequency domain values.

Phase Nonlinearity is the deviation of phase response from a perfect linear-phase response as a function of frequency.

Signal-to-Noise and Distortion Ratio (SINAD) is defined for a pure sine wave input of specified amplitude and frequency, as the ratio of the root mean square (*rms*) amplitude of the analog-to-digital converter output signal to the *rms* amplitude of the output noise,

where noise is defined as above to include not only random errors but also nonlinear distortions and the effects of sampling time errors.

Total harmonic distortion (THD) is defined for a pure sine wave input of specified amplitude and frequency, as the root sum of squares (*rss*) of all the harmonic distortion components including their aliases in the spectral output of the analog-to-digital converter. Unless otherwise specified, THD is estimated by the *rss* of the 2^{nd} through the 10^{th} harmonics, inclusive. THD is often expressed as a decibel ratio with respect to the root mean square amplitude of the output component at the input frequency.

In order to evaluate this factor of the merit the following calculation should be made:

$$THD = \frac{1}{M}\sqrt{\sum_{h} X_{avm}(f_h))^2} \tag{11}$$

where, $X_{avm}(f_h)$ is the averaged magnitude of the component at the h^{th} harmonic of the DFT of the ADC output data record and M is the number of samples in the data record.

When measuring the THD, an extra care should be taken by using DFT transforms, and thus a correct using of windowing should be done in order to reduce the analysis noise.

Intermodulation Distortion (IMD) is defined similar to what is done for amplifiers and so will not be further described here, more information on this can be seen in [40] for a precise definition of these schemes. Again an extra care should be taken in these measurements since they are done using the well known DFT.

Multi-tone Intermodulation Distortion (MT-IMD) is defined similar to what is done for amplifiers, but in reference [25] nothing is said about how to generate this type of stimulus, since the phase relationship between each of the tones, will impose different signal statistics and thus different peak-to-average ratios [41], which can generate completely different values of distortion at the output of the ADC.

Chapter 3

System Level Concepts

In this section a brief explanation of the main concepts related with the system level analysis point of view are presented. The signal information is introduced in terms of Probability Density Function (PDF), Complementary Cumulative Distribution Function (CCDF) and multisine signals distributions. Next some concepts about bandpass sampling (also called undersampling) are presented. Moreover, a brief review of Peak-to-Average Power Ratio (PAPR) is show, because this is one of the most important figures of merit in the actual SDR solutions. Finally, the most important causes of nonlinear distortion in SDR receivers are analyzed in depth.

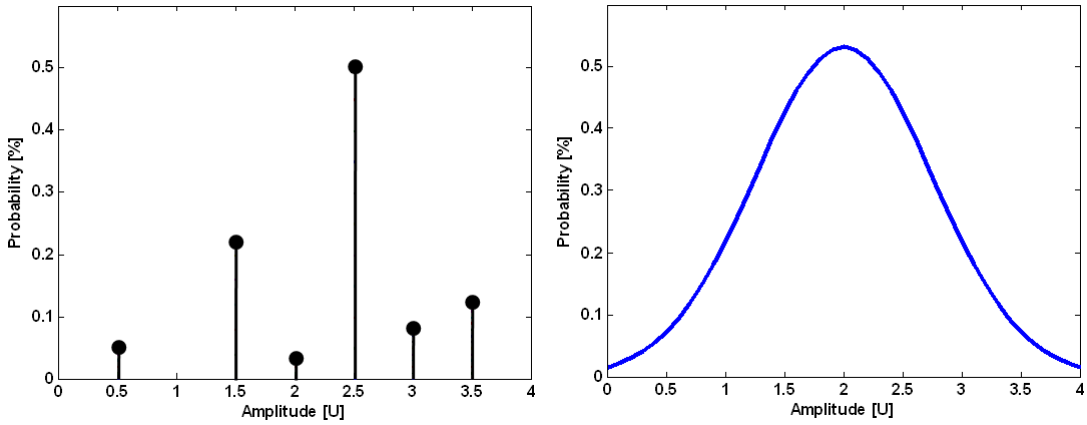
3.1 Signal Information

In every wireless communication system is essential to use some concepts about probability functions. This knowledge is important in the characterization of the channel that the wireless signal traverses, in the design of system components (amplifiers, ADC, DAC, etc) and in the evaluation of the RF front ends.

Several books are devoted to the subject of random processes and probability, [42, 43]. Here, only a brief review about PDF, CCDF and common signal distributions is done.

3.1.1 Probability Density Function

Every random variable *x* is characterized by a probability density function, *pdf(x)*. The PDF is established after a large number of measurements have been performed, which determine the likelihood of all possible values of *x*. A discrete random variable possesses a discrete PDF (Fig. 22 (a)), on the other hand a continuous random variable possesses a continuous PDF (Fig. 22 (b)).



(a) (b)

Fig. 22 – Simulated (a) discrete PDF and (b) continuous PDF

There are two important properties for PDFs. First, no event can have a negative probability. Thus,

$$pdf\,(x) \geq 0 \tag{12}$$

Second, the probability that an x value exists somewhere over its range of values is certain. Thus,

$$\int_{-\infty}^{+\infty} pdf\,(x)dx = 1 \tag{13}$$

Both properties must be satisfied by any PDF. Since the total area under the PDF is equal to 1, the probability of x existing over a finite range of possible values is always less than 1.

Considering, yet the PDF, this one can be used to obtain several properties of a random variable *x*. The most obvious property is the statistical average that is defined as the expected value. Thus, the expected value of *x* is:

$$E[x] = \int_{-\infty}^{+\infty} x.pdf\,(x)dx \tag{14}$$

The random variable *x* in the previous equation can also be any function of *x*, *f(x)*. So, the expected value of *f(x)* is:

$$E[f(x)] = \int_{-\infty}^{+\infty} f(x).pdf\,(x)dx \tag{15}$$

The expected value of *x* is typically called the moment of first order and is denoted as:

$$m_1 = \int_{-\infty}^{+\infty} x.pdf\,(x)dx \tag{16}$$

Then, the moment of n^{th} order is defined as:

$$m_n = \int_{-\infty}^{+\infty} x^n.pdf\,(x)dx \tag{17}$$

If the random variable is expressed in volts, the moment of first order will correspond to the average (mean or dc voltage) and the moment of second order corresponds to the average power.

3.1.2 Complementary Cumulative Distribution Function

Complementary Cumulative Distribution Function (CCDF) curves provide critical information about the signals used in actual communications systems. Theses curves show how much time the signal spends at or above a given power level, i.e., gives a statistical description of the power levels in the signal.

First is presented the statistical origin of CCDF curves, next their importance in communications systems components is introduced with some examples.

As was explained in [44] the statistical origin of the CCDF curves comes from the PDF. Consider the signal shown in Fig. 23 and the respective distribution function variation with the amplitude, Fig. 24.

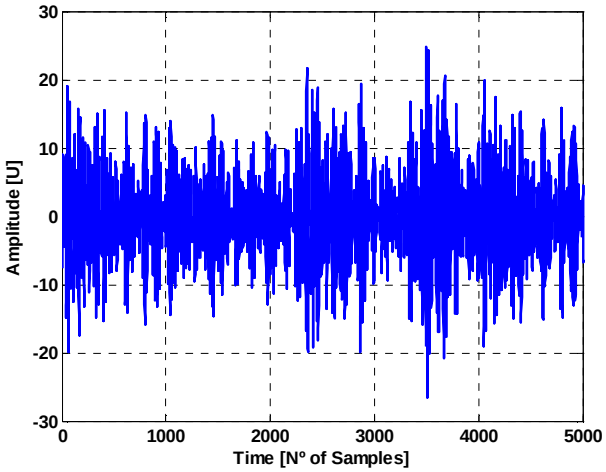


Fig. 23 - Time-domain sample signal

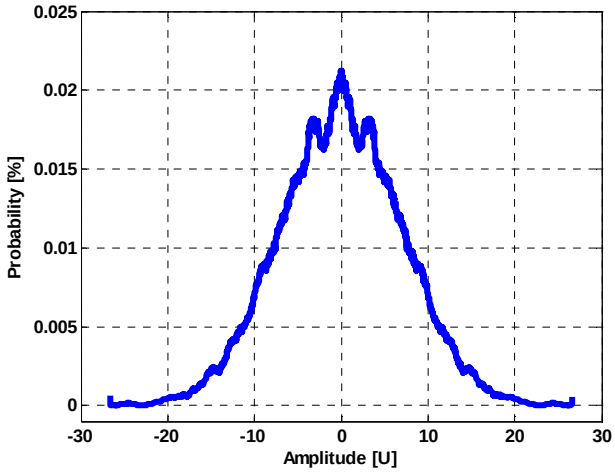


Fig. 24 - Respective PDF of previous signal

Then, the Cumulative Distribution Function (CDF) can be related to the PDF by:

$$CDF(x) = \int_{-\infty}^{a} pdf(x)dx \tag{18}$$

Finally, knowing that the CCDF is the complement of the CDF (i.e., CCDF = 1 – CDF) this gives the result presented in Fig. 25.

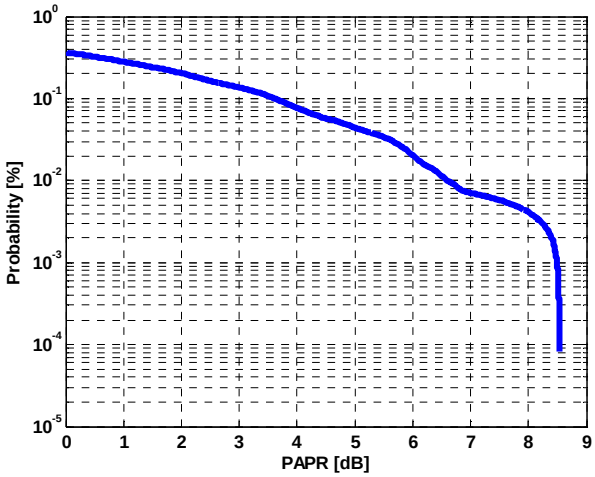


Fig. 25 - Respective CCDF of previous signal

Several degradations of the transmitted/received signals can be analyzed using the CCDF curves. Next figure presents the variation of Peak-to-Average Power Ratio (PAPR, explained in chapter 3.3) of a GSM signal using one and three channels. As can be seen, the complexity of the three GSM channels significantly degrades the overall signal, Fig. 26.

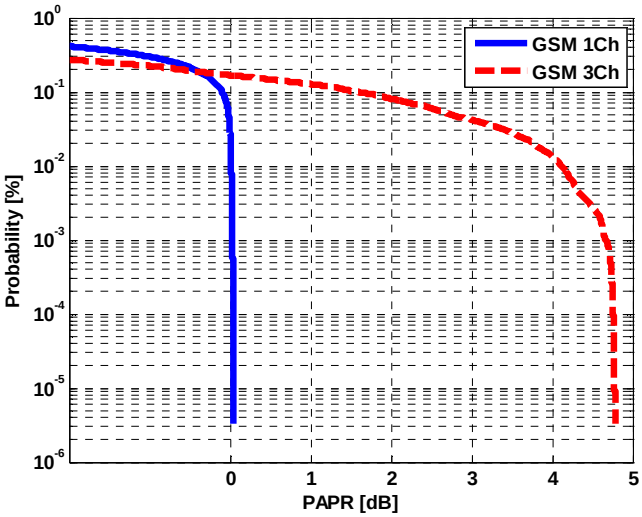


Fig. 26 - CCDF curves for a GSM signal with 1 Channel and 3 Channels

Other item that has impact in PAPR is the modulation format. Fig. 27 presents the PAPR for two modulation formats (QPSK and 64-QAM).

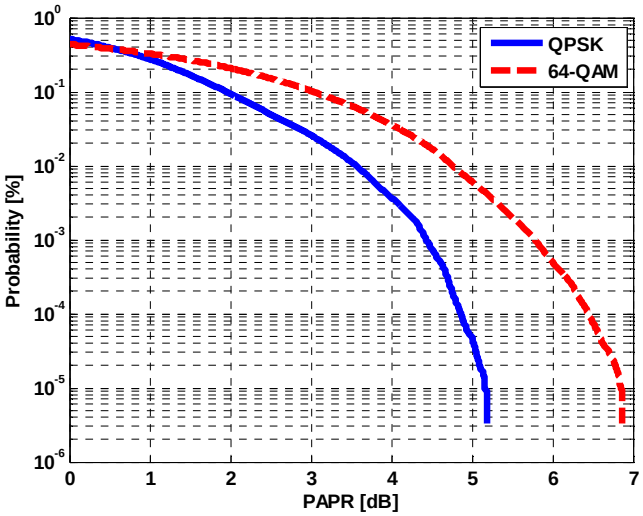


Fig. 27 - CCDF curves for QPSK signal and 16-QAM signal

Analyzing the previous figure can be concluded that the RF components used for a 64-QAM signal will have different design needs than those for QPSK signal.

So, CCDF curves are a very important tool in the design and testing of system components as amplifiers, mixers, converters, etc.

3.1.3 Multisine Distributions

The use of some common multisine signals is intended to approximate digitally modulated excitation, as was basically demonstrated in [45]. This type of signals consists of a summation of discrete-time sine-waves, typically with constant frequency spacing, Δf, between them. They are much easy to generate than digital modulation and characteristics such as PAPR are simple to control. A bandpass multisine can be represented by:

$$x_{MS}(t) = \sum_{k=0}^{N-1} A_k . \cos(2\pi(f_c + k.\Delta f)t + \phi_k) \tag{19}$$

where, f_c is the carrier frequency, Δf is the spacing between the several tones and N is the total number of tones.

The different magnitude A_k and phase Φ_k of each sine-wave allows the generation of different behavior multisines. So, in order to evaluate the behavioral model proposed (in chapter 4), several multisines with different arrangements had to be constructed.

Two common distributions was chosen, which are the uniform and normal (gaussian) distributions. Another, which is identified as Constant Phase, has joined and this have the relative phase difference between the tones equal to 0º and the several magnitudes are always fixed at one. The Constant Phase multisine is the worst case possible, and even though that it is only used in academia tests, we want to evaluate this particular case.

Next, the functions of the first two distributions mentioned above are presented. The normal probability density is perhaps the most common *pdf*, and can be defined as:

$$pdf(x) = \frac{1}{\sqrt{2\pi\sigma^2}} . e^{-(x-\mu)^2/2\sigma^2}, \qquad -\infty \le x \le +\infty \tag{20}$$

where, μ is the mean value and σ^2 is the variance.

On other hand, the uniform probability density is also much used, and this is defined as:

$$pdf(x) = \frac{1}{b-a}, \qquad a \le x \le b \tag{21}$$

where, the mean value can be shown to be $\frac{(a+b)}{2}$ and the variance approximately $\frac{(b-a)^2}{12}$.

3.2 Bandpass Sampling

In this chapter some concepts about bandpass sampling, that is the intentional aliasing of the information bandwidth of the RF signal, are addressed. This capability is one of the main characteristics of the actual used ADCs as pipelined and successive approximations (SAR) [46].

The Nyquist sampling theorem states that if a signal is sampled at least twice as fast as the highest sampled frequency component, no information will be lost when the signal is reconstructed. One popular technique used in analog to digital conversion is known as bandpass sampling, which is the intentional aliasing of the information bandwidth of the

signal [47-48]. The sampling frequency requirement is based on the bandwidth of the signal, rather than in the frequency of the RF carrier.

The spectrum can be divided in several zones, called Nyquist Zones. The Nyquist frequency is Fs/2, which can vary depending on the sample rate (Fs) and the frequency range from DC to Fs/2 is known as the first Nyquist Zone and so on, Fig. 28.

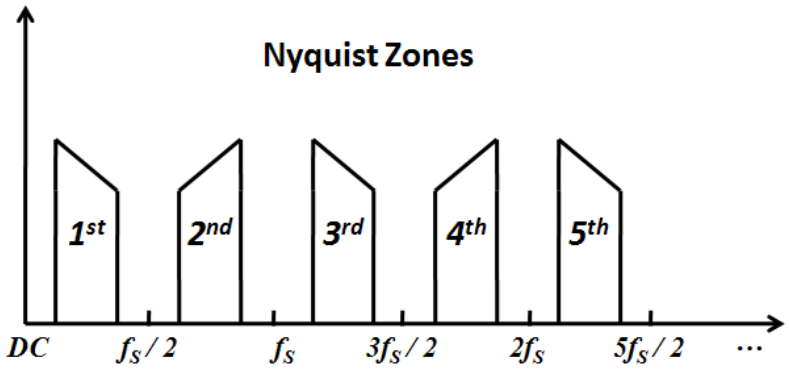


Fig. 28 - Spectrum divided in several Nyquist zones

The concept of Nyquist Zones is only true into the full power bandwidth (FPBW) of the ADC. The FPBW of an ADC is the range of frequencies from DC to the point at which the spectral output of the fundamental frequency (determined by DFT analysis) is reduced by 3dB. The characteristics of the ADC are frequency sensitive and tend to degrade as the input frequency is increased [49].

This technique has the advantage of the sampling frequency and consequent processing rate are proportional to the information bandwidth rather than the carrier frequency. However, one critical requirement is the necessity of use a bandpass filter with bandwidth equal to the information bandwidth of the signal and centered in the RF carrier or a filter that selects each one of the Nyquist Zones, so that the entire FPBW of the ADC does not fold into the resulting pass band, the first Nyquist zone.

3.3 Peak-to-Average Power Ratio

Peak-to-Average Power Ratio (PAPR) is a relationship between the maximum value of the peak power and the average power of the signal, see expression (22) and Fig. 29.

$$PAPR = \frac{\max_{0 \le t \le NT} |x(t)|^2}{1/NT \int_0^{NT} |x(t)|^2 \, dt} \tag{22}$$

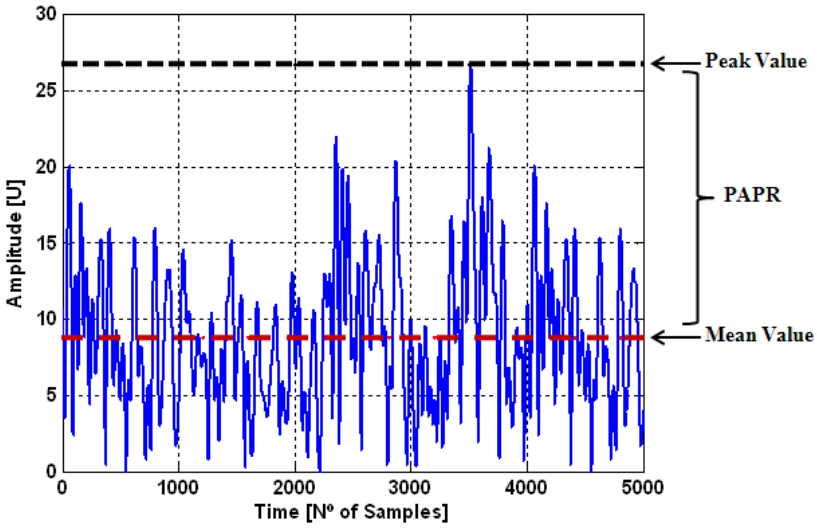


Fig. 29 - Time-Domain of a sample signal where the PAPR is explained

The evaluation of the impact of PAPR in the communications systems is mainly made through the analysis of CCDF curves (explained in chapter 3.1.2) that provides a statistical description of the power levels in the signal. Next figure presents the respective CCDF curve for the signal of Fig. 29.

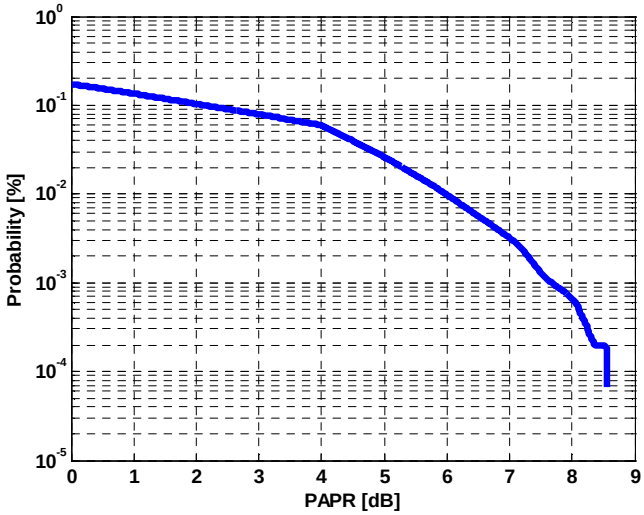


Fig. 30 - CCDF curve of the previous signal

In actual SDR solutions [9] the receiving and transmitter stages should deal simultaneously with all the multi-standard to operate and thus increasing the dependency with the PAPR signals.

In most of today standards the Orthogonal Frequency Division Multiplexing (OFDM) has been adopted due to its spectral efficiency and capability to transmit high data rates over broadband radio channels. But the conjugation of both multi-norm systems and OFDM based schemes will lead to high values of PAPR, which limits the power that can be received or transmitted without distortion as can be seen in [50].

This PAPR problem immediately degrades the quality of the transmitted and received signal, either by the fact that we should use high values of input power back off in power amplifiers degrading its efficiency or by the fact that PAPR impose a degradation of SNR in the receiver. On the other hand, if we allow the clipping of the signals peak then immediately the nonlinear distortion rises.

PAPR reduction techniques have been proposed along the times and they span from software to hardware techniques. Those include techniques based on coding [51], partial transmit techniques [52], tone reservation [53], active constellation extension [54], tone injection [55] and amplitude clipping/filtering [56]. When these techniques are applied a great care should be taken since the PAPR can be reduced without much ACPR degradation, but other problems may appear like an increase in the Bit Error Rate (BER).

3.4 Nonlinear Distortion Causes in SDR Receivers

Purely digital SDR receivers will be composed mainly of a LNA stage and an ADC, which will convert the RF analog signal immediately to the digital domain. It is expected that the nonlinear distortion arising in this type of receiver will come from a combination of the nonlinear behavior of both the LNA and the ADC. Thus, these two components will be studied, first independently, and then in a model that describes the complete black-box SDR receiver distortion.

3.4.1 Low Noise Amplifier Causes

An RF/microwave low-noise amplifier can be made from single or multiple transistor configurations. An example of the latter case is shown in Fig. 31. The input matching network is tuned for low noise and the output matching network is tuned for maximum gain. The transistor is then biased to a single voltage where the noise figure is minimized. Nevertheless the drain (collector) current of the transistor is a nonlinear function of the gate voltage (base current) and thus, will impose nonlinear distortion on the circuit response.

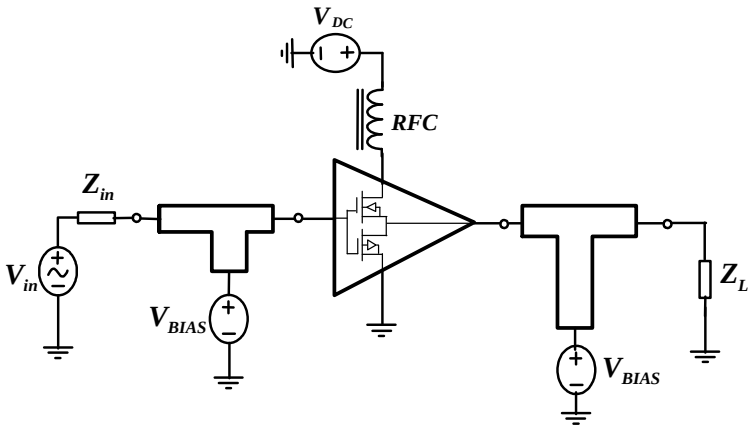


Fig. 31 - Typical LNA circuit based on field-effect transistors, FETs

If the transistor is to be used in a narrowband LNA, then it will operate most of the time as a small-signal device. That is, the input signal will be a small excitation relative to the bias point. However, if utilized in a high-bandwidth LNA for receiving diverse input signals, then the transistor may operate in a large-signal mode. This is because some of the signals present at the input port can block small-signal ones. Such a combination of several input signals can degrade the PAPR of the input signal.

Much has been written about nonlinear distortion in small-signal amplifiers, for instance in [57]. Here, we will retain only the more important characteristics relevant to SDR applications.

In small-signal operation, nonlinear behavior is often approximated by a simple polynomial. For instance, the Taylor series of the output current versus the input voltage may be used if the transistor can be considered memoryless (that is, if all distortion

products arise from RF effects, not ones related to baseband-frequency effects). For systems with memory, a Volterra-series analysis can be considered, since it will incorporate dynamic, baseband effects and thus will approximate more conveniently the behavior of the LNA small signal distortion. Expressions (23) and (24) present this relationship.

$$y(t) = \sum_{n=1}^{\infty} y_n(t) \tag{23}$$

Where,

$$y_0(t) = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \cdots, \tau_n) * x(t - t_1) \cdots x(t - t_n) d\tau_1 \cdots d\tau_n \tag{24}$$

Here, are considered that $h_n(\tau_1,\ldots, \tau_n)$ is the n^{th} order Volterra kernel, and *x(t)* is the input signal waveform.

In large-signal operation, the transistor starts to clip the output signal due to the fact that it will compress and saturate when the output current swing reaches the breakdown and/or the knee voltage of the transistor, as shown in Fig. 32. This behavior can be approximated by a large-signal transfer function, often by a describing function approach [40, 57], Fig. 33.

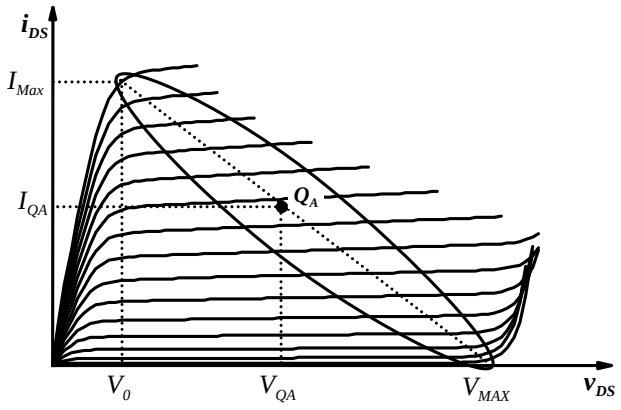


Fig. 32 - Typical DC current/voltage curves of a FET

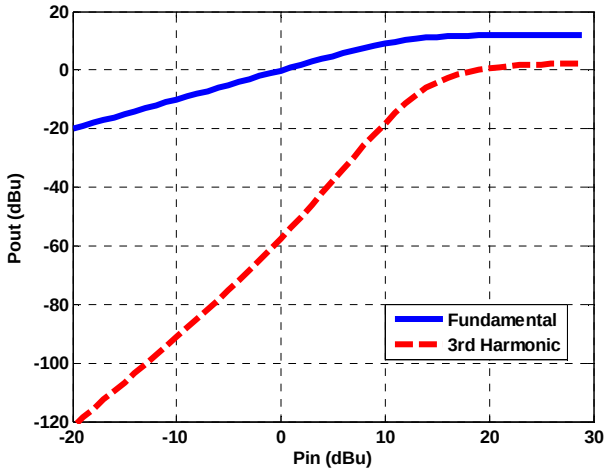


Fig. 33 - Simulated compression behavior and nonlinear distortion of an amplifier under large-signal RF excitation

Thus, for the LNA the most important sources of nonlinear distortion are the small-signal behavior of the drain current versus gate voltage, and under large-signal operation, the compression due to the maximum operation conditions of the transistor.

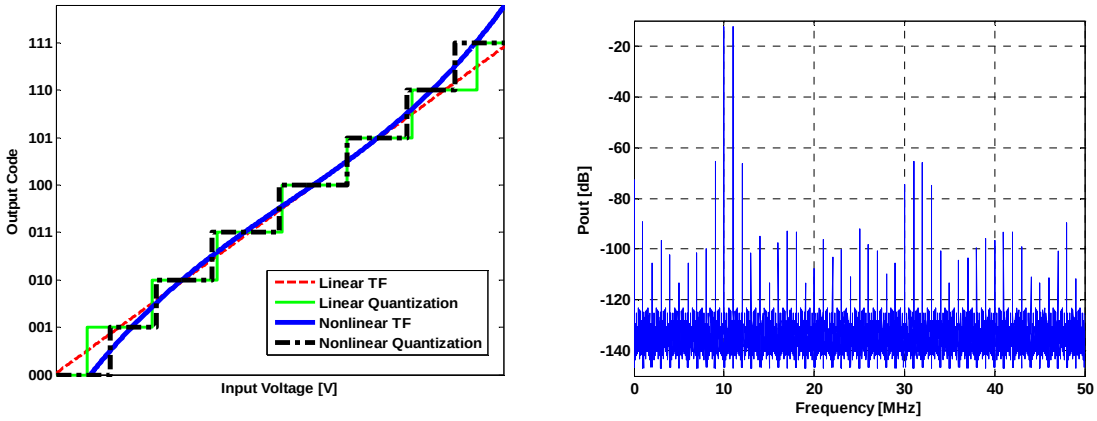
3.4.2 Analog-to-Digital Converter Causes

A second important component with respect to nonlinear distortion in an SDR is the ADC [25]. The ADC is a more complex entity than the LNA, since it doesn´t have the same sources of distortion as were found in the LNA, but additional sources as well. Following, is shown an individually explanation about the mechanisms that create nonlinear distortion.

3.4.2.1 Nonlinear Transfer Function

One of the sources of nonlinearity in an ADC is the nonlinearity of its transfer function, as illustrated in Fig. 34 (a). This nonlinearity can be responsible for missing bits, and subsequent integral nonlinearity (INL) and differential nonlinearity (DNL). This nonlinear behavior can be efficiently modelled by using a polynomial function (followed by an ideal quantizer), and thus is similar to the small-signal distortion behavior of the LNA.

The nonlinearity of the ADCs transfer function gives rise to the generation of higher values of harmonic distortion and intermodulation distortion (IMD). Fig. 34 (b) illustrates this effect, by plotting the IMD at the third harmonic of the fundamental frequency when the nonlinear behavior of the ADC transfer function is highly nonlinear. In this case the transfer characteristic was represented by a polynomial function.



(a) (b)

Fig. 34 - Simulated (a) nonideal ADC transfer function and (b) its corresponding nonlinear distortion pattern in the frequency domain

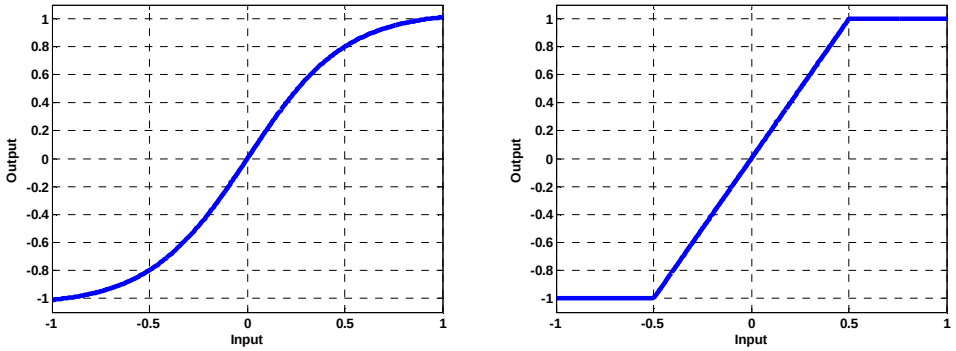
3.4.2.2 Clipping

Another source of distortion common to ADCs is related to the maximum voltage that the ADC can digitize without clipping. If the ADC transfer curve is overdrive this will generate harmonics of the input signal. This distortion is amplitude dependent and is of great importance in many new wireless communication systems due to the high PAPR of their signals.

This form of clipping is what is termed hard clipping and is imposed by a transfer function that limits the output signal right after the input signal traverses a certain threshold. This is different from the soft clipping imposed by the transfer function of the LNA, where the signal starts to clip smoothly. Fig. 35 presents the difference between hard and soft clipping.

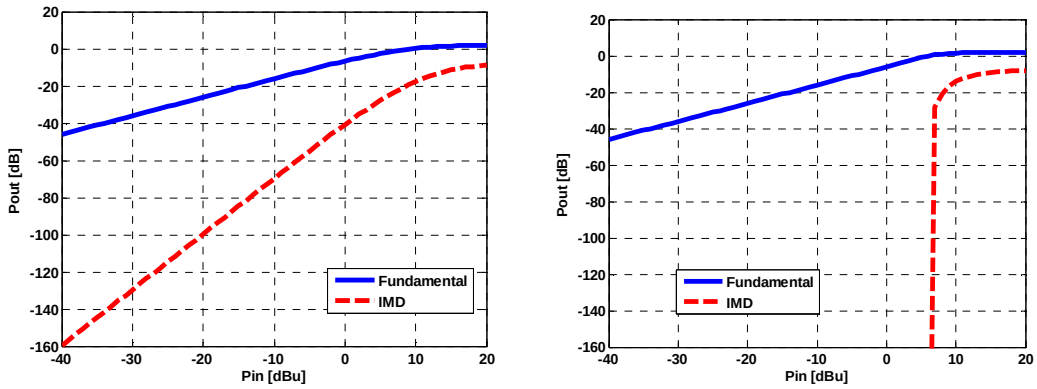
Note that ADC manufacturers always specify the valid operating range of their products. However, in a real SDR scenario we do not known a priori what signals will be

received. Thus, the PAPR may be quite different from what is expected, and it may change rapidly. One solution is to reduce the gain at the input of the ADC and avoid clipping, but then the output will be corrupted by noise. Another solution is to allow some ADC clipping even though this will generate some amount of distortion.



(a) (b)

Fig. 35 - Simulated (a) soft clipping and (b) hard clipping functions



(a) (b)

Fig. 36 - Simulated nonlinear compression for the corresponding clipping functions, (a) soft and (b) hard

Fig. 36 shows that even though the output signal power and the distorted signal (harmonics) tend to a similar value, the behavior is completely different. In the case of soft clipping small-signal distortion is always presents, while in the case of hard clipping, no small signal distortion is visible. This is due to the fact that hard clipping only happens if the signal traverses the ADCs maximum voltage range. Moreover, the signal and the distorted replica compresses to a constant value. This can be explained by the fact that in

the limit the output signal will tend to a square wave. This is visible in Fig. 37, where the output of an ADC under sinusoidal excitation is shown. Waveform 1 is the output signal under small-signal excitation and Waveform 2 is the output under large-signal excitation.

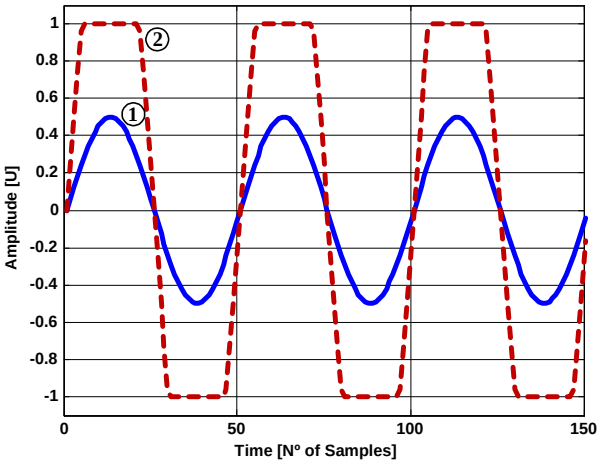


Fig. 37 - Clipping effect on a sinusoidal function

If the signal that excites the ADC clipping function is a complex, modulated signal, then the PAPR of the excitation will impart different patterns on the clipping saturated value. In order to understand this behavior, a multisine wave was used when its time-domain statistical behavior approximates a uniform probability density function, or the case of constant, aligned phases, as illustrated in Fig. 38.

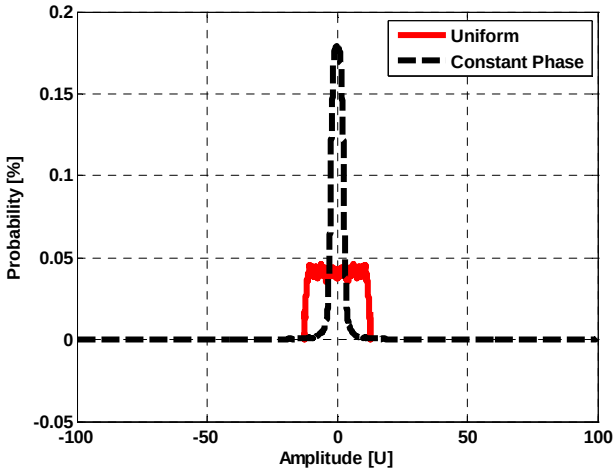
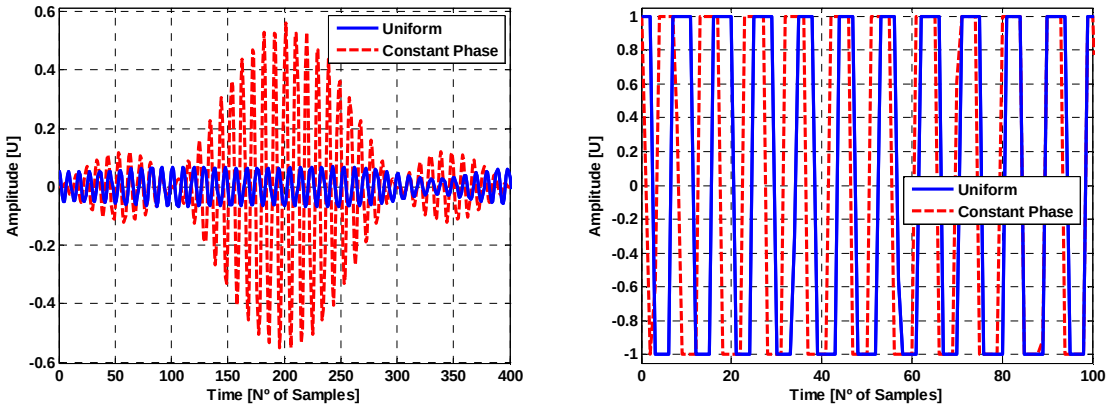


Fig. 38 - PDF function of multisines having uniform (solid) and constant-phase (dashed) distributions

The time-domain statistics of a multisine excitation will produce different time-domain output waveforms. Fig. 39 (a) shows the simulated time-domain waveforms for the two multisines presented above, when the multisines passed in linear regime and Fig. 39 (b) when they are severely clipped. Moreover, should be noted that both signals have the same integrated power over one envelope cycle, but in the graphs the time-domain waveform was truncated.



(a) (b)

Fig. 39 - Simulated output voltage waveforms of multisines having uniform (solid) and constant-phase (dashed) distributions, in (a) linear regime and (b) severely clipped

Fig. 40 presents the output power for both multisines and for the case where the RF is a pure square-wave function. The constant-phase multisine starts to clip at a lower input power due to the fact that its higher voltage peaks are cut sooner than the low-value peaks of the uniform signal. However, as the input power increases, the uniform multisine output power tends rapidly to a saturated value. This is due to the fact that its time-domain waveform characteristic moves rapidly to a square wave function once clipping occurs. That is, most of the uniform multisines time-domain waveform clips simultaneously, while in the constant-phase case most of the signal waveform has a low value compared with its peaks. On average the constant-phase multisine will be clipped at a higher input power level, which means that the signal will saturate smoothly compared to the previous one, Fig. 40.

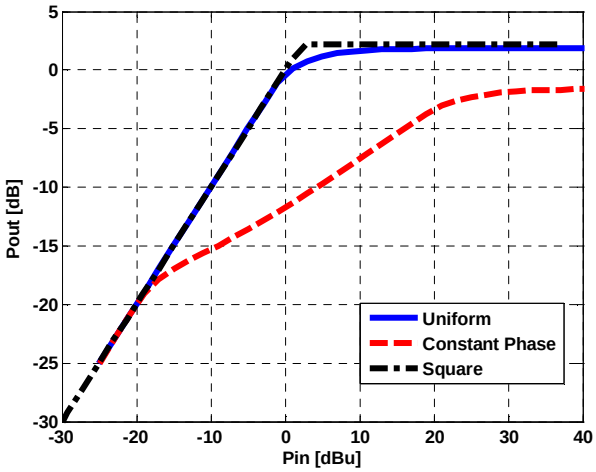


Fig. 40 - Output power as a function of input power applied to a simulated ADC

Fig. 40 shows that the signals do not clip to the same saturated output power. This can be explained by considering that the input power can be calculated by the moment of second-order of the probability density function (PDF) of the input signal (more detail in chapter 3.1.1).

$$P = m_2 = \int_{-\infty}^{+\infty} x^2 . pdf\,(x) dx \tag{25}$$

The output will thus be

$$P = \int_{-\infty}^{+\infty} y^2 . pdf\,(y) dy \tag{26}$$

We used the property that

$$pdf\,(y) = \frac{pdf\,(x)}{\left|\frac{dy}{dx}\right|} \tag{27}$$

If the clipping function is the hyperbolic tangent function, *tanh(x)*, then can be written:

$$P = \int_{-\infty}^{+\infty} \tanh^2(x) \frac{pdf\,(x)}{\sec h^2(x)} dx = \int_{-\infty}^{+\infty} \sinh^2(x)\, pdf\,(x) dx \tag{28}$$

Because $\sinh^2(x)$ is zero at $x = 0$, and tends asymptotically to infinity, it is expected that the signals presenting a higher-valued PDF near zero will have a lower value of saturated

power than the ones that do not present this behavior. Thus, looking back to Fig. 38, the constant-phase multisine will be the one that saturates to a lower value of output power, since its probability of occurrence is concentrated near zero.

3.4.2.3 Quantization

The remaining source of nonlinear distortion in an ADC is the well-known quantization process. This highly nonlinear operation also gives rise to a high value of interference called quantization noise.

Quantization changes a sine wave from a smooth function to a staircase signal, as illustrated in Fig. 41. Due to this nonlinear effect, the output signal is composed of a large number of nonlinear distortion products. For instance, if a sine wave is used at the input, then the output will be the sine wave itself followed by all of its harmonics, that arise mainly from the quantization effects on the input signal.

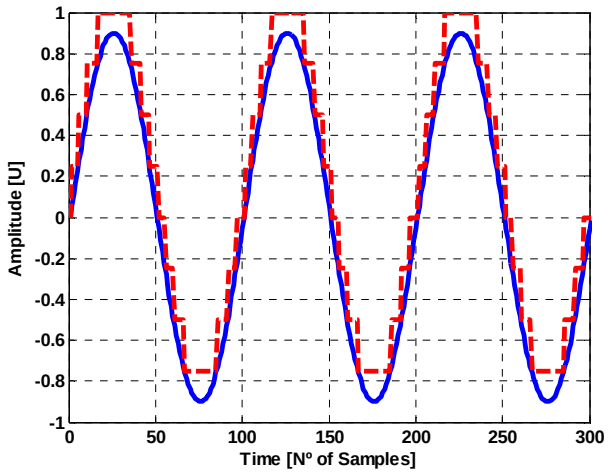


Fig. 41 - Analog sine wave signal (solid) and its quantized version (dashed)

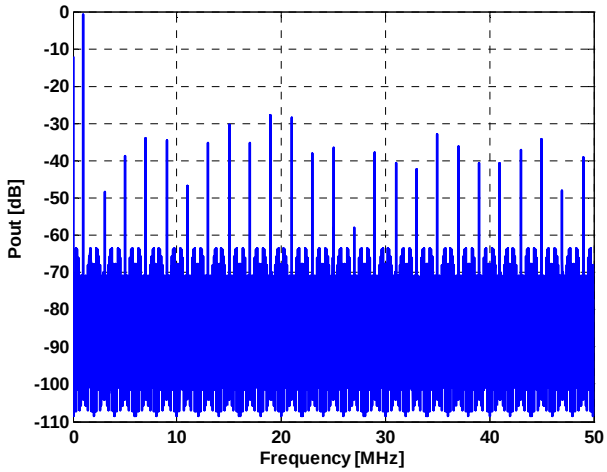


Fig. 42 - Simulated spectrum of a sine-wave signal at the output of an ideal quantizer

Fig. 42 presents the output spectrum of a quantized sine-wave signal. There are some clearly delineated spectral lines that correspond to the harmonics of the 1 MHz fundamental due to the nonlinear behavior of the quantizer. These spectral lines can further be correlated or uncorrelated to the input signal clock.

In order to understand this mechanism, the quantization and sampling mechanism will be considered combined.

The sampling mechanism is a linear scheme, since the output signal represents the input signal at certain selected (sampled) points. An example is shown in Fig. 43, where we represent a real sampling process applied to the input signal. Here, the initial sampled points are oversampled using a sample and hold system.

As can be seen a staircase is also visible, but ideally the process is completely linear since for the sampled points, the input signal and the output signal are equal.

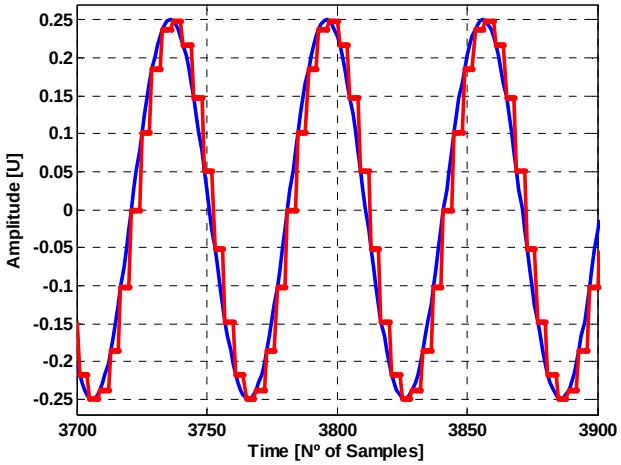


Fig. 43 - Output signal after ideal linear sampling

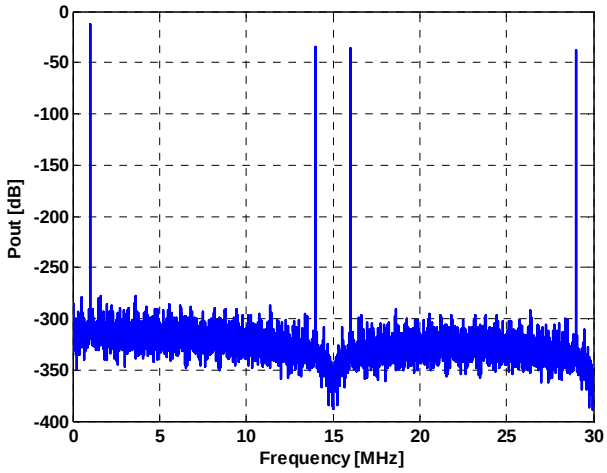


Fig. 44 - Signal spectrum after ideal linear sampling

In Fig. 44 a spectral line at 1 MHz can be seen, corresponding to the input signal. The lines at higher frequencies correspond to the oversampling mechanism arising from the digital sample and hold system.

The quantization process will then round each quantized value up or down according to the quantization pattern. This nonlinear operation gives rise to the so-called quantization error that was been explained in chapter 2.2.1 and where is shown that the SNR of a digitized signal can be easily approximated by expression (8).

As can be seen this noise (quantization) is due to the fact that the output is not equal to the input, but it is a staircase equivalent signal. Because the nonlinearity due to quantization is so severe the number of harmonics is quite large and replicas will be

generated over an extremely wide bandwidth (spanning over the sampling rate). In Fig. 42 we can see those harmonics.

In this evaluation a clear distinction could also be made between the two types of signal components: those correlated with input signal with the sampling clock, and those uncorrelated with input signal with the sampling clock.

If the clock (RF clock sampling) that is used in the sampling process is related to the input signal (coherent sampling) then all of the harmonics will fall on top of each other. In this case, the value of each harmonic will increase, since it is nothing more than the summation of all the harmonics.

$$P_{harm}(\omega_i) = \sum_{k=1}^{+\infty} P_{ord}\left[i + \frac{\omega_n}{2}(k-i) \right] \tag{29}$$

where $P_{ord}(x)$ is the power of the nonlinear order x, i is the harmonic to calculate and w_n is the sampling frequency.

On the other hand, if the clock is not related to the input signal, incoherent sampling, the harmonics will spread over the entire sampling bandwidth and the spectral lines will be reduced, since they will not fall on each other. Thus, they will not add. Next figures present three different cases of this problem.

The first case involves coherent sampling (Fig. 45), where the clock is fixed at 100 MHz and the input frequency is 1 MHz. Here, the harmonics will fall exactly on top of each other.

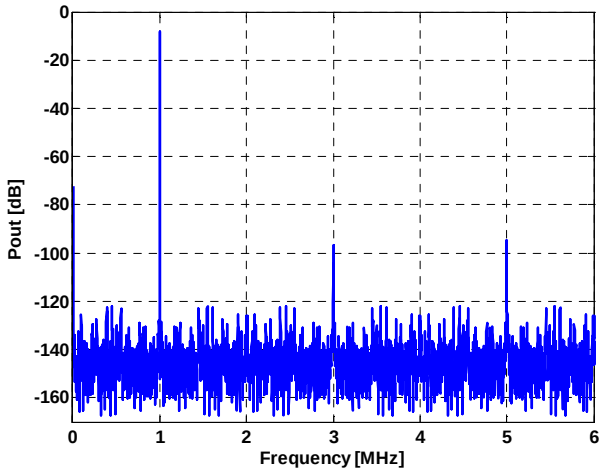


Fig. 45 - Simulated signal spectrum for coherent sampling clock

In the second case (Fig. 46), partially incoherent sampling is considered, where the input frequency is 1.1 MHz. In this case, very few harmonics are a multiple of the sampling period, so they form a large set of spectral lines.

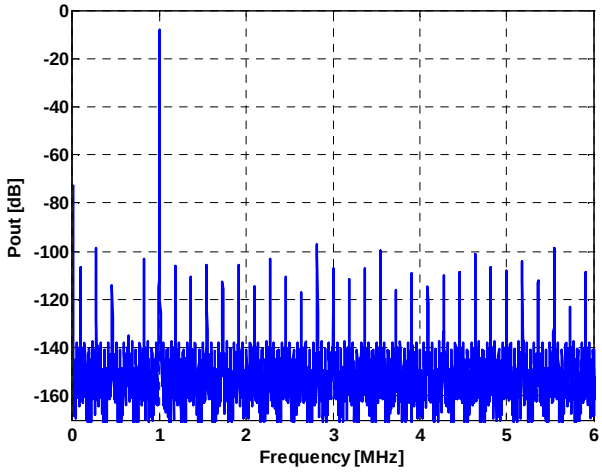


Fig. 46 - Simulated signal spectrum for partially incoherent sampling clock

Finally, the case of a completely uncorrelated sampling clock is simulated (Fig. 47), where the harmonics will never fall on top of each other and will spread over the entire spectrum. For the latter case, the spectral lines will fall at frequencies of:

$$\omega = \mathrm{mod}\left(k\omega_f, \frac{\omega_n}{2} \right), \quad k \in \{1 \cdots \infty\} \tag{30}$$

where w_f is the fundamental frequency of the input signal and mod is the modulus after division.

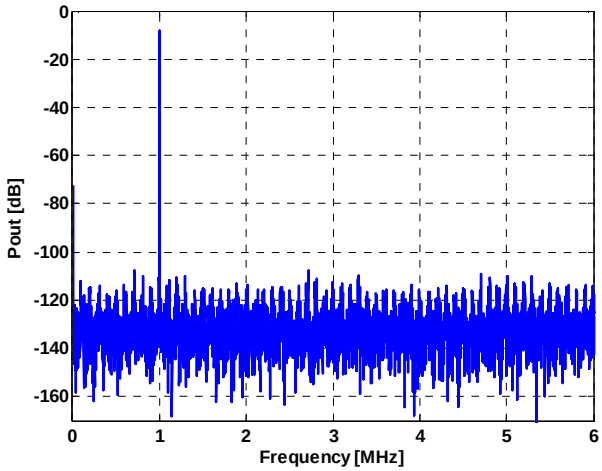


Fig. 47 - Simulated signal spectrum for uncorrelated clock

Circuit designers often artificially create incoherent sampling by adding in a certain amount of noise (also called dither) to the input signal, see Fig. 48. In this way, an improved spectral spread is obtained [58]. It should be clear that in all situations the quantization process was due to a nonlinear process of the input sine wave.

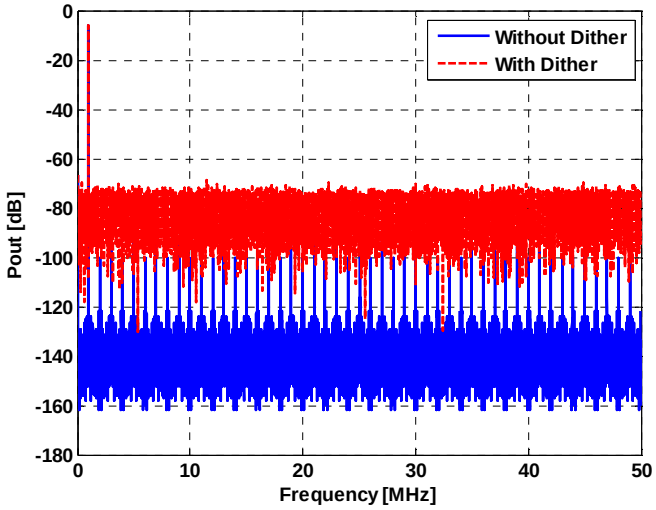


Fig. 48 - Dither in a quantized signal

Another interesting calculation that can be done is to obtain the SNR for each previous case. In the first case, the quantization noise is condensed into the signal harmonics, which means the harmonics are representative of the generated noise. In the second case, the harmonics fall in different positions of the spectral grid, according to equation (30), so the noise calculation is based on all these lines. In the third case the entire spectrum should be used, since the lack of correlation between the clock and the input signal means that the noise covers all frequencies.

As can be seen from Table 1, the SNR is approximately equal in all situations to the previous calculation of (7), as was expected.

Table 1: Simulated SNR for each type of sampling

Type of Sampling	**Simulated SNR [dB]**
Ideal result from (7)	74
Coherent Sampling	73.33
Incoherent Sampling	73.83
Uncorrelated Clock	73.65

The quantization error will further be reduced if the number of bits increases, and thus the rounding error will be minimized as the nonlinear function gets smoothed. This is also visible from expression (8). The value of each spectral line can also be calculated precisely as was done in [59, 60]. If we have a very high sampling rate, then similar approaches such as those used in sigma-delta quantizers, could also be used. This is equivalent to the smoothing of the quantization pattern.

Chapter 4

Behavioral Model for SDR Evaluation

In order to be able to describe most of the previous sources of nonlinear distortion, a bandpass behavioral model will be built that represents the nonideal behavior of the SDR front end architecture. The first block of the model that will be used is the small-signal model to represent the nonlinearity of the LNA and the ADC transfer function. This is represented by a Volterra series approximation. The large-signal operation of both components is represented by a clipping function that could be described by a hyperbolic tangent or any other limiting function [61].

The signal is then ideally sampled and then ideally quantized. Here, is considered that the nonlinear behavior due to the non-monotonic performance of the ADC will be included into the Volterra series. Since, the overall system is measured from the output terminals the information on individual nonlinearities inside the system is not available. Fig. 49 presents the proposed behavioral model of the SDR front end description.

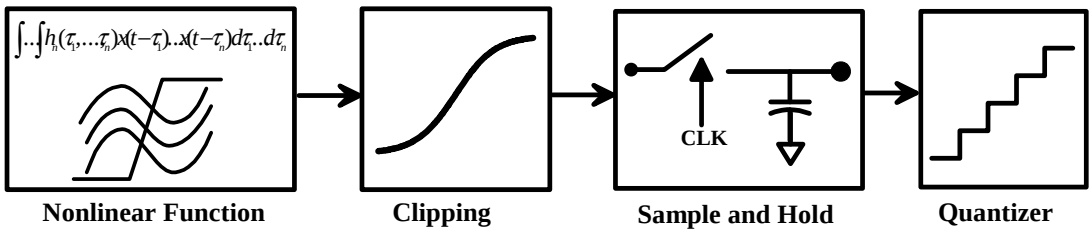


Fig. 49 - Proposed behavioral model for the SDR front end receiver

A model is only good if the extraction and model development procedures are quite simple and efficient. In this model, the polynomial (Volterra) parameters can be extracted by using small-signal measurements. For the third-order nonlinear descriptor, will be used the zone of the third-harmonic output where the distortion power rises at three decibels per decibel.

The compression of the nonlinear distortion, and the fundamental signal power, will define the parameters of the hyperbolic tangent or other clipping function. Finally, the quantization and sampling block is imposed by the ADC used in the SDR front end.

The measurement set-up that was been used for the parameter extraction and for the measurements [62] is described in chapter 5.

4.1 Model Extraction from Real Measurements

It is important to refer that in all of the measurements that was been made, is used a SDR receiver (Fig. 50) constituted by a commercially LNA and a commercially 12-bit pipeline ADC. Also, that the carrier frequency of the signals is in the 3rd Nyquist Zone and a bandpass filter was used to avoid aliasing of other signals present in the FPBW of the ADC, which is approximately 750MHz. The clock frequency used was 100 MHz because some limitations of the equipment used.

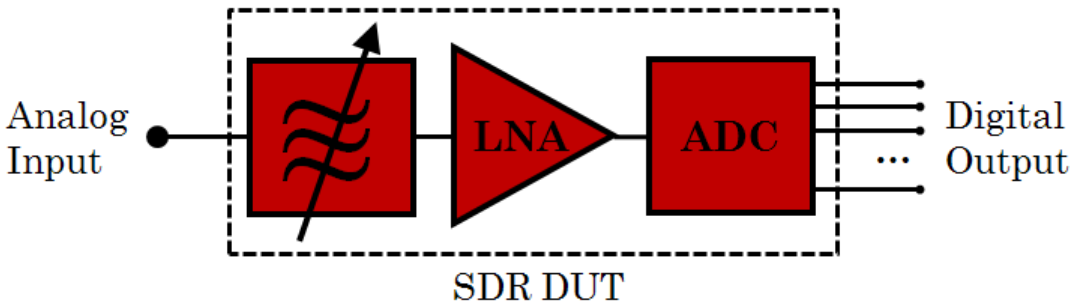


Fig. 50 – Configuration of the SDR receiver front end used in the measurements

In order to extract the proposed model, a one-tone signal was used as the excitation. Fig. 51 presents the measured results for the fundamental and third-harmonic frequencies.

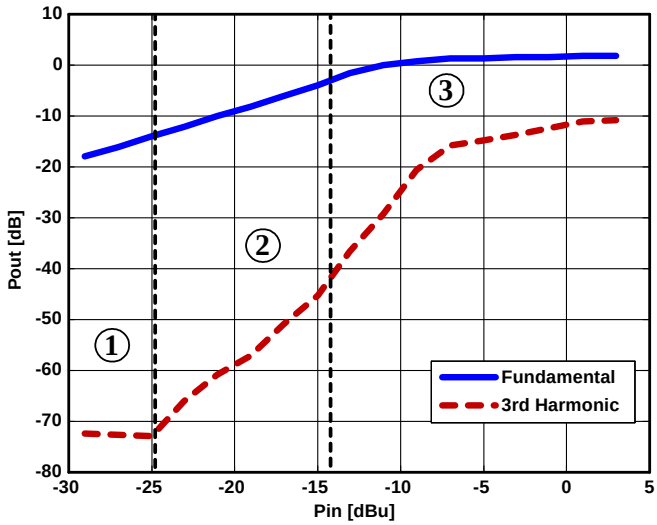


Fig. 51 - One-tone measurements of the output power as a function of the input power from an SDR front end

In Fig. 51, three different zones may be identified. The first zone is eliminated for parameter extraction since the harmonics that were sought are lower than the measured noise level. From the second zone, where the third-harmonic distortion rises at three decibels per decibel of input power, the third-order coefficient is extracted. Finally, the value that will be used to select the clipping breakpoint is extracted from the third zone, where the fundamental signal is near its 1 dB compression point. To model large signal operation a hyperbolic tangent was used as the clipping function.

This extraction procedure allows us to have a first estimate of the coefficients. Then, a least-square function is used to minimize the difference between measured and simulated results for the model based on the one-tone extraction.

Through additional experiments, was observed that this SDR front end behaved as a memoryless system, since the coefficients did not change significantly with frequency. This means that the Volterra series could have been approximated by a simple polynomial. If this was not the case, then a two- or three-tone excitation should have been used for the parameter extraction and to identify the Volterra nonlinear operators [63].

In order to confirm that this model can describe the behavior of an SDR front end under modulated-signal excitation were carried out measurements when a two-tone signal was applied to the input, and compared the output values with our modelled results.

Fig. 52 presents the obtained results for the output fundamental and the third-order IMD values. Good agreement can be seen between the measurements and the simulations.

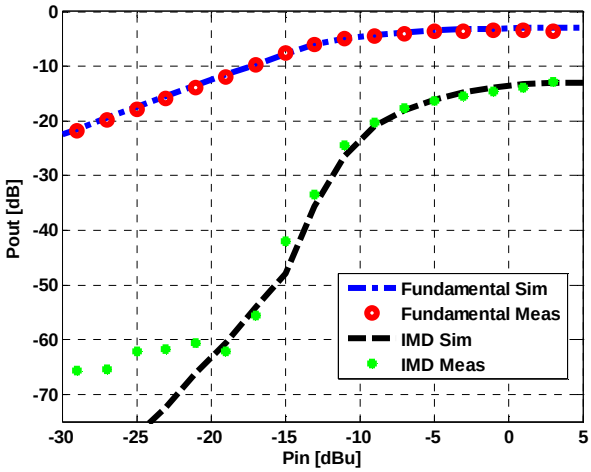


Fig. 52 - Two-tone measurements and simulations comparing the output power at the fundamental and the third-harmonic frequencies

A sweep of the spacing between the two tones was also made, but was observed very little difference with tone spacing compared to the results in Fig. 52. This confirms that the measured front end is essentially memoryless. The observable difference between measured and simulated third-harmonic results at low input-power levels is due to the noise floor of the measurement set-up used.

4.2 Validation with Complex Modulated Signals

Two different tests were conducted in order to provide additional validation of the proposed behavioral model and to better understand the impact of a real SDR front end on complex modulated signals. The first test used an excitation signal consisting of a multisine with different PAPR arrangements [41]. The second test used an excitation signal based on the WiMax standard [64].

4.2.1 Evaluation with Multisines

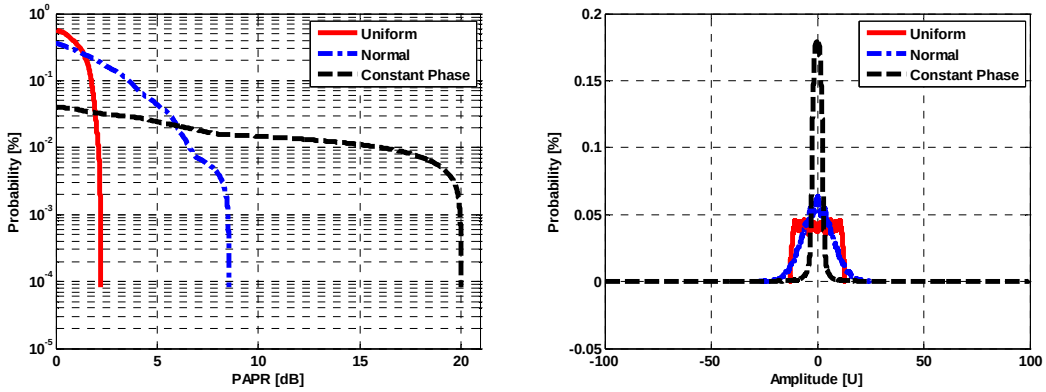
For the test using the multisine waveform, several amplitude/phase arrangements for the frequency components of the multisines were used in order to mimic different time-domain-signal statistics and thus PAPR. In this case, several 100-tone multisines with a

total occupied bandwidth of 1 MHz were used. Table 2 presents the different values of PAPR for each multisine arrangement.

Table 2: Measured PAPR for each excitation signal

Signal Type	PAPR [dB]
Uniform	2.1266
Normal	8.5184
Constant Phase	20.0000

Fig. 53 presents the measured statistics for each multisine arrangement. The Constant Phase arrangement is the one where the relative phase difference was 0º between the tones. This yields a large value of 20 dB PAPR. As can be seen from Table 2, the PAPR varies significantly with the engineered statistics of the multisine. The different amplitude/phase arrangements allow the generation of a time-domain uniform, normal or constant phase statistical behavior, but with the same integrated power.



(a) (b)

Fig. 53 – Measured (a) CCDF and (b) PDF functions for three different 100-tone multisines

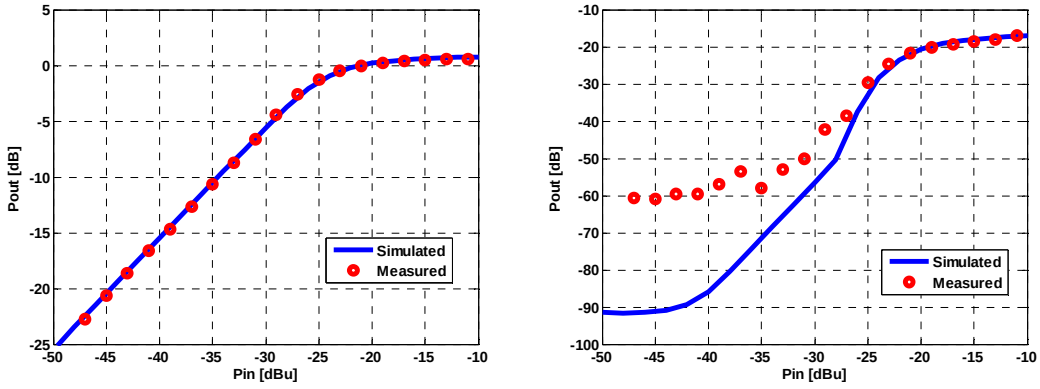
Next figures present the measured and simulated results. Fig. 54 shows the total power at the excitation frequencies (a) and the total power in the adjacent channel (b) for uniform distribution. Fig. 55 and Fig. 56 present the same results for the normal and constant phase distributions, respectively.

The signal with constant-phase statistics deviates from linearity at a much lower input power level than for the other cases since the PAPR of that signal is extremely high and so clipping occurs at a relatively low input level, as discussed in Section 3.4.2.2. As well, the

adjacent channel power is significantly higher for the constant phase case than for the others.

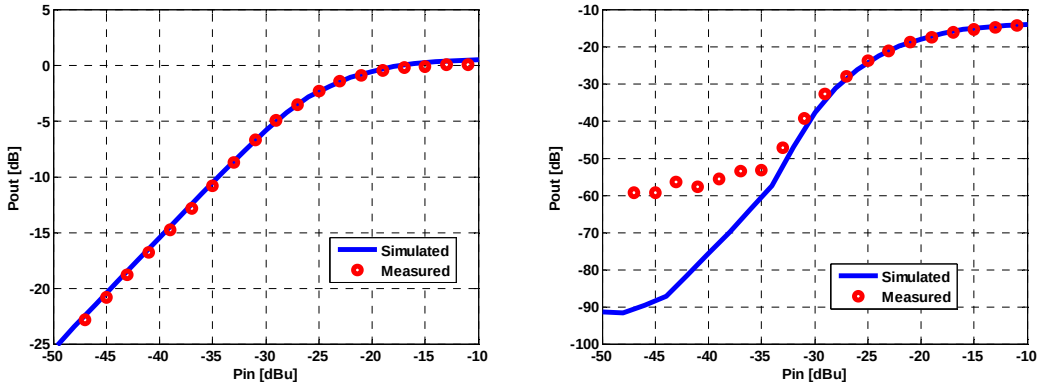
Under small-signal excitation the SDR front end is mainly ruled by quantization noise in the simulations and by noise in the measurements. Then the distortion starts to rise for medium-signal excursions at three decibels per decibel input power. At high input power levels, it compresses to a saturated value. In the constant-phase scenario (Fig. 56 (a) and (b)), the input power still does compress due to the reasons described in Section 3.4.2.2.

The good match between the simulations and the measurements shown in the figures indicates the viability of the proposed model for nonlinear description of an SDR front end.



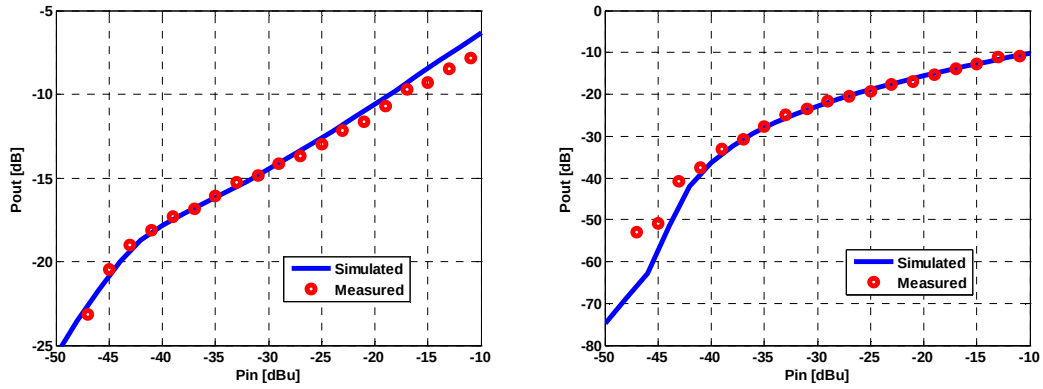
(a) (b)

Fig. 54 - Measured and simulated results with uniform multisine, (a) fundamental power and (b) ACPR distortion



(a) (b)

Fig. 55 - Measured and simulated results with normal multisine, (a) fundamental power and (b) ACPR distortion

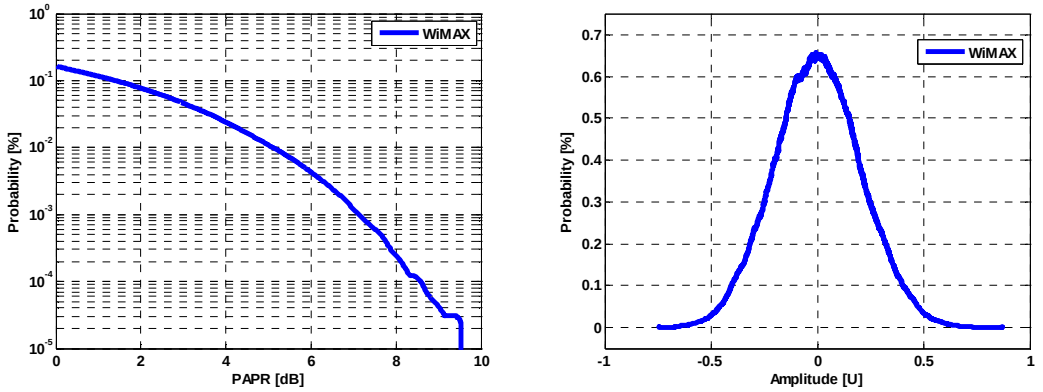


(a) (b)

Fig. 56 - Measured and simulated results with constant phase multisine, (a) fundamental power and (b) ACPR distortion

4.2.2 Evaluation with WiMax Excitation

In this section, a WiMax signal [64] was used as the SDR front end excitation. This one consists in a single-user WiMax signal in frequency division duplex (FDD) mode with a bandwidth of 3 MHz and a modulation type of 64-QAM (¾), Pseudo-Random Binary Sequence (PRBS-11) sequence. This was generated using a vector signal generator [65]. Fig. 57 presents the CCDF and the PDF of this signal and Table 3 presents the obtained PAPR for this signal. Again, the measurement system outlined in Fig. 60 was used, where the output signal data were acquired by a logic analyzer and post processed to provide the measured results shown.



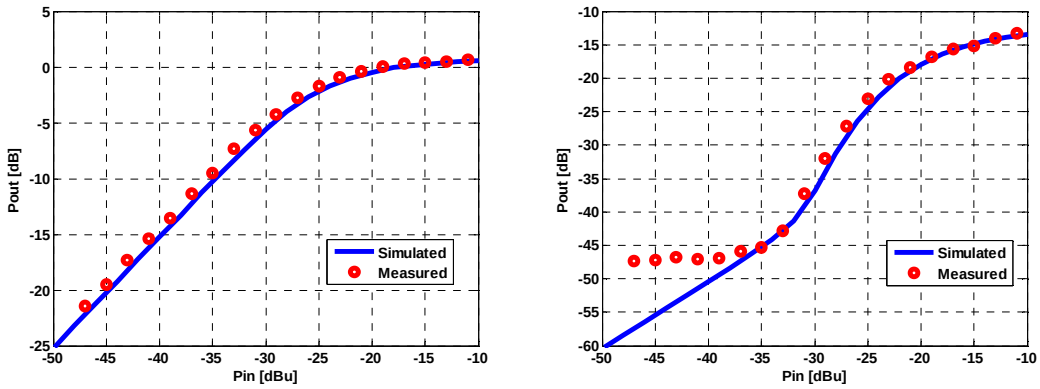
(a) (b)

Fig. 57 - Measured (a) CCDF and (b) PDF functions for WiMax excitation

Table 3: Measured PAPR for WiMax excitation signal

Signal Type	PAPR [dB]
WiMax	9.5266

Measured and simulated results are presented in Fig. 58. Again, a good agreement between measured and simulated results can be seen. The higher noise floor for the WiMax signal when compared to the multisines shown in previous chapter comes from the fact that the arbitrary waveform generator that was used for the WiMax signal produced a significant amount of noise.



(a) (b)

Fig. 58 - Measured and simulated results with WiMax excitation, (a) fundamental power and (b) ACPR distortion

Chapter 5

Instrumentation for SDR Characterization

Software-defined Radios (SDRs) typically utilize both analog- and digital-domain signals. For receiver front ends, the input is analog and the output is digital. For transmitters such as class S amplifiers [66], the input is digital and the output analog. Instrumentation that is normally used for analog components does not typically provide enough information to characterize the system adequately since much of the signal exists only in the digital domain.

Here, is proposed a mixed-domain instrument that allows the user to evaluate simultaneously the overall radio path, from analog to digital domains. Also, is proposed techniques for synchronization of the acquired signals and describe how to time align the two types of measured signals.

Key parameters of the digital domain measurements include non-idealities such as offset/gain error, INL and DNL [25], for more detail see chapter 2.2.3. In the analog domain important figures of merit include VSWR, gain, etc [67].

5.1 SDR Instrumentation

As was referred previously, measured quantities such as those already used to quantify analog measurements continue to be valid in SDR, for instance, input VSWR, gain, bandwidth, nonlinear effects, etc. Thus, the same approach as was used for standard analog

instrumentation will be followed here, developing a concept similar to an analog/digital S parameter. Fig. 59 presents the fundamental concept for this type of instrument.

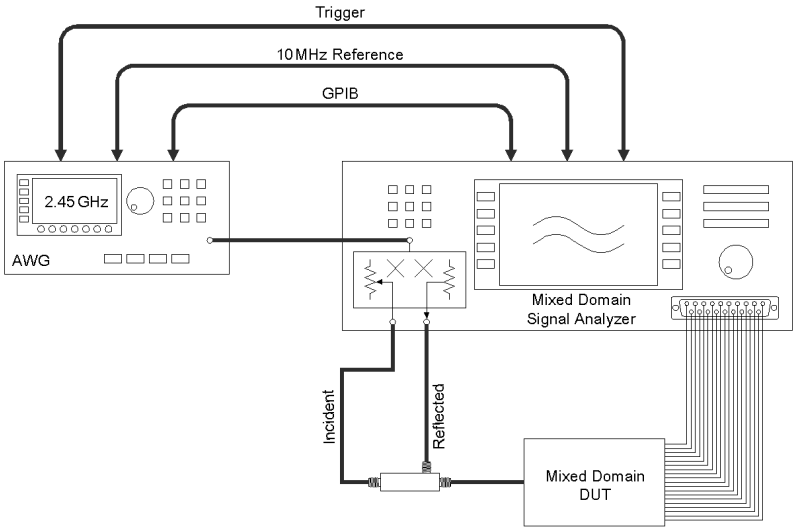


Fig. 59 - Mixed-domain instrumentation in which an arbitrary waveform generator (AWG) excites the mixed-domain DUT

As seen in Fig. 59, the analog channel has the channel configuration of a network analyzer, while the second channel is a digital channel, where the input signals are no longer analog ones, but are actually bit sequences. This will allow us to measure important information such as the reflection coefficient at the input port, since:

$$\rho(\omega) = \frac{V_{ref}(\omega)}{V_{inc}(\omega)} = S_{11D}(\omega) \tag{31}$$

where $V_{inc}(w)$ and $V_{ref}(w)$ are the incident and the reflected waveforms at port 1 (analog signal) and S_{11D} is an analog S parameter. Thus similar quantities can thus continue to be defined in this scenario as the $S_{21D}(w)$ which allows the measure of "gain" of the DUT from an RF point of view.

Other important information related to amplitude and phase change can now be gathered. For instance, the linear transfer function relating input to output signal is given as

$$H_L(\omega) = \frac{V_{dig}(\omega)}{V_{inc}(\omega)} = \frac{\frac{1}{T}\int_{-T/2}^{T/2}[2^{n_1(t)} + \cdots + 2^{n_N(t)}].V_{ref}.e^{-j\omega t}dt}{\frac{1}{T}\int_{-T/2}^{T/2} v_{inc}(t).e^{-j\omega t}dt} \quad (32)$$

This format can also be used to compute other forms of nonlinear transfer functions, such as those for systems containing all-analog components. Such transfer functions can be based on higher-order statistics for nonlinear distortion evaluation [68].

In fact, what we are measuring is nothing more than a time-domain signal, whether in the analog or in the digital domain. The need to time align signals measured with this instrument is the same as for quantities that were measure using analog instrumentation.

External alignment signals should continue to be used, including GPIB, trigger, and signal reference, since those will be determinant on the time alignment of the overall signals. The next section presents one possible implementation of this ideal vision by using regular laboratory instrumentation.

5.2 Laboratory Implementation

In order to implement the mixed-domain instrument using a feasible laboratory arrangement, a version using individual measurement equipment was assembled, that is presented in Fig. 60.

As shown in the next figure, for the analog part a time-domain instrument was used, such as an oscilloscope or a microwave transition analyzer (MTA). In the other hand, to sample the signals in the digital domain a logic analyzer was used.

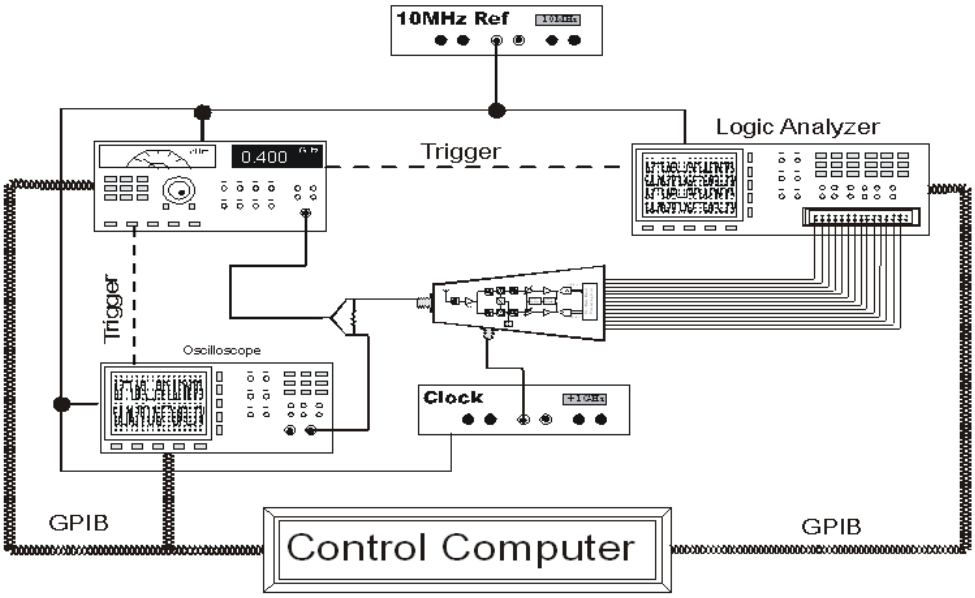


Fig. 60 - Laboratory setup of a mixed-mode instrument

These two systems are then synchronized using a common 10 MHz reference and a trigger signal that allows time synchronization between signals. This step is done because the input and output signals will be measured at different times and they should be synchronized afterwards in post processing.

Even though the same sampling frequency is used for both instruments, extra care should be taken for the correct selection of this quantity. If different sampling frequencies are used for the analog scope, the digital scope, and for the DUT, then interpolation and/or decimation should be done carefully in order to guarantee a similar time base for all the signal components.

In the case implemented, similar sampling frequency of 20 MHz was used for all the instruments. Also, should be guaranteed that all the signals are synchronous, that is measuring the signal at the same instant of time.

5.3 Triggering Mixed Mode Signals

One extremely complex problem to resolve in a measurement system like the one that is proposed is how to synchronize all the different measured signals. In the laboratory measurement set-up that were used doesn't have synchronized samplers, even though they

are all locked to a 10 MHz reference and that are used external trigger sequences whenever possible. The synchronization of all the signals is a fundamental problem that must be resolved if the phase relationships between the input and output signals want to be extracted.

The need for external synchronization has driven us to propose the use of an excitation signal that consists of a triggering pulse embedded in the input signal followed by the waveform excitation of interest; for instance, a sinusoidal tone, a two-tone, or a multisine signal (see Fig. 61). Methods such as this were proposed in [68, 69].

The process of triggering starts by generating a signal in the arbitrary waveform generator that includes a first triggering sequence followed by the waveform to be measured. This signal is generated by first creating the complex envelope waveform, sampled at 20 MHz. This in-phase/quadrature (I/Q) envelope signal is then downloaded to the generator and up-converted to the selected output frequency. The signal is then sampled both at the analog and digital scopes during different time intervals by means of an external trigger that was previously configured in the generator as an external marker.

The measurement process starts by selecting one of the sampled waveforms as the reference waveform, and then referring all the previous waveforms to that reference. For small-signal operation, for instance, a replica of the trigger signal can be extracted.

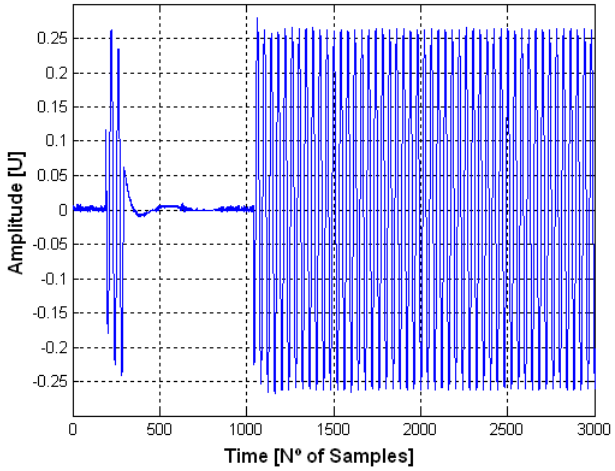


Fig. 61 - Excitation waveform including the triggering sequence initial pulse

Then in subsequent measurements we correct the trigger signal at the MTA and at the logic analyzer to the reference trigger. This way, all the signals will be synchronous. In each measurement, the first n_{trg} points with the same amplitude are reserved for the signal

trigger. Then the generated waveform is corrected according to that trigger and its first periods are deleted in order to eliminate any transient arising from the change of the trigger sequence to the waveform itself. The remaining signal will be the input and output measurement sequence.

5.4 Measurement Examples

In order to clearly show how this instrument can be usefully applied in a laboratory environment, an SDR receiver was used. This SDR receiver front end is similarly to that used in the behavioral model (chapter 4), which consists of a LNA followed by an 8-bit pipeline ADC with a sampling clock of 20 MHz. This sampling clock was chosen because exists some restrictions in the laboratory equipment used.

The first measurement was the equivalent transfer function of the overall system as given in equation (32). The amplitude and phase change of the output signal was measured for a sinusoidal input signal.

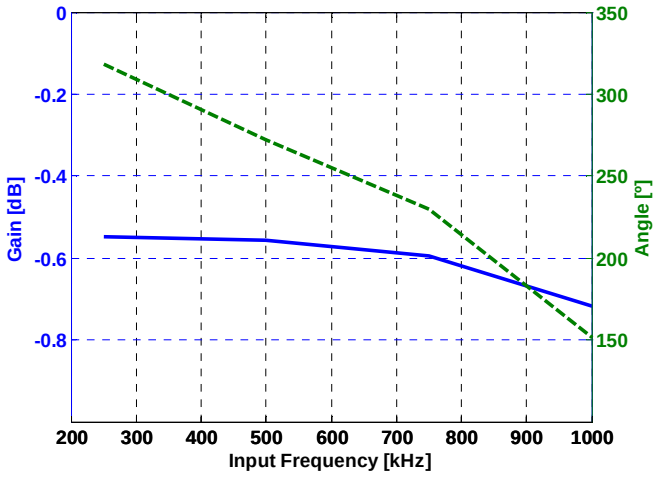


Fig. 62 - Transfer function of an SDR when the input signal was swept in frequency, gain amplitude (solid) and phase difference (dashed)

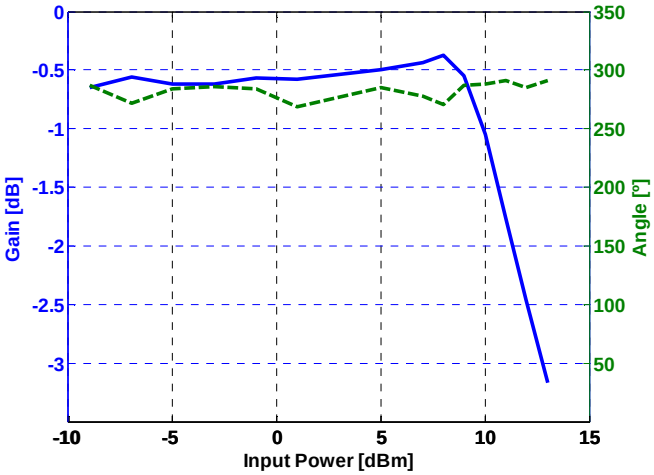


Fig. 63 - Transfer function of an SDR when the input signal was swept in power, gain amplitude (solid) and phase difference (dashed)

As seen in Fig. 62, the output amplitude is almost constant with frequency, and the phase decreases almost continuously. Then, a swept in the input signal amplitude was done considering a fixed frequency, as shown in Fig. 63. These curves represent the AM/AM and AM/PM values, as would be seen in a power amplifier characterization.

Finally, a two-tone test was performed. Fig. 64 presents the first-order transfer function and the third-order intermodulation distortion nonlinear transfer function for the two-tone case, where the input power was swept and the distortion products plotted. In addition, Fig. 65 presents the respectively phase variations with the input power for first-order and third-order.

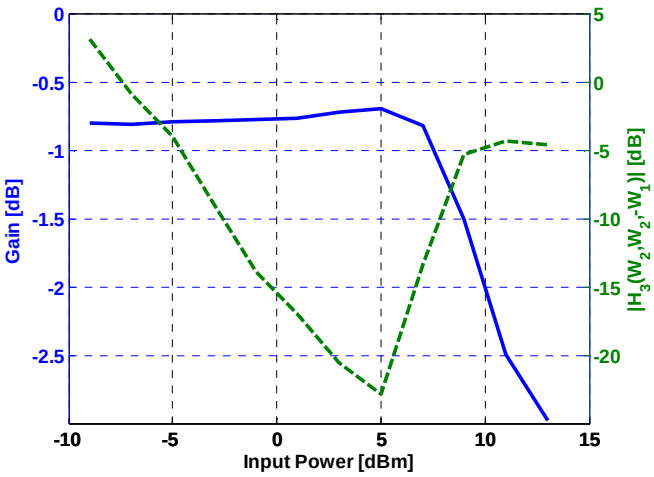


Fig. 64 - First-order (solid) and third-order (dashed) transfer functions

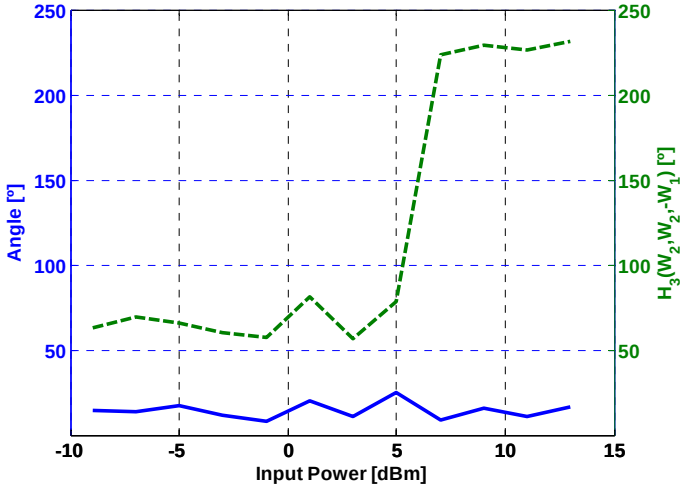


Fig. 65 - Phase of the first-order (solid) and third-order (dashed) intermodulation distortion product relative to the output phase of the fundamental and the corresponding ideal third-order distortion

Chapter 6

Conclusions

In this dissertation an evaluation of nonlinear distortion mechanisms in Software-defined Radio front end receivers was presented in detail, either caused by the LNA or by the ADC, which are two main components of an ideal SDR solution.

It was seen that the nonlinear distortion can be a concern in systems developed for high PAPR signal handling. In that respect a behavioral model was also proposed for the SDR nonlinear distortion characterization.

The performance of this model was compared to measurements of two-tones, multisines and complex modulated excitation as WiMax signal. Also, was noted that the SDR front end used can be considered memoryless.

The good agreement between the simulations and the measurements confirm that the proposed model represents well the main observed characteristics.

In this work a new mixed-domain, analog-digital, instrument that is specially tailored to the characterization of SDR systems was also presented. The idea that was addressed here utilizes typical laboratory equipment in the implementation.

Signal timing, synchronization requirements was also discussed and possible solutions, like including a trigger sequence in the measurement signal were presented.

6.1 Future Work

In order to improve the results obtained in this dissertation it is necessary to evaluate the impact of an ideal SDR receiver, as the one used here, in important parameters of some communications systems (e.g. GSM, UMTS and WiMax). For instance, estimate parameters like Error Vector Magnitude (EVM) or Bit Error Rate (BER) in systems that use complex modulated signals as QPSK or x-QAM.

Other important enhancement is the study and development of PAPR reduction techniques in order to diminish it impact in SDR receivers as the one used here.

It is mandatory to assess the proposed behavioral model when the SDR receiver is subject to various multi-mode signals, since these radios theoretically will digitize the entire spectra and thus the impact in PAPR value of several multi-mode signals is a very demanding and important problem.

Relating to the proposed measurement system there are some important problems that still have to be addressed, including the development of a calibration procedure and error analysis of measurements made with such systems.

Is also very interesting to export the studies carried on in this dissertation to the transmitter chain and evaluate the results.

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Caracterização de Sistemas para Software Defined Radio

Autor: Pedro Miguel Cruz

Orientador: Prof. Nuno Borges Carvalho

Universidade de Aveiro 30 de Julho de 2008

Sumário

- Software Defined Radio Ideal (Conceito)
- Distorção num Receptor de SDR
- Modelo Comportamental do SDR
  - Resultados Obtidos
- Instrumentação Proposta
- Conclusões

Sumário

- Software Defined Radio Ideal (Conceito)
- Distorção num Receptor de SDR
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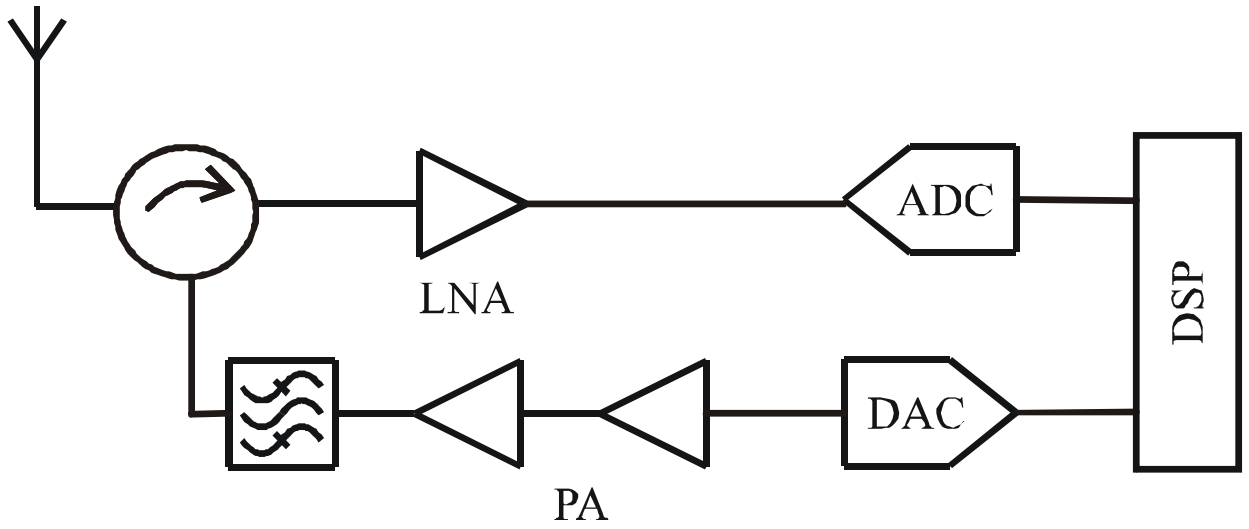
- Conclusões

SDR Ideal (Conceito) – I

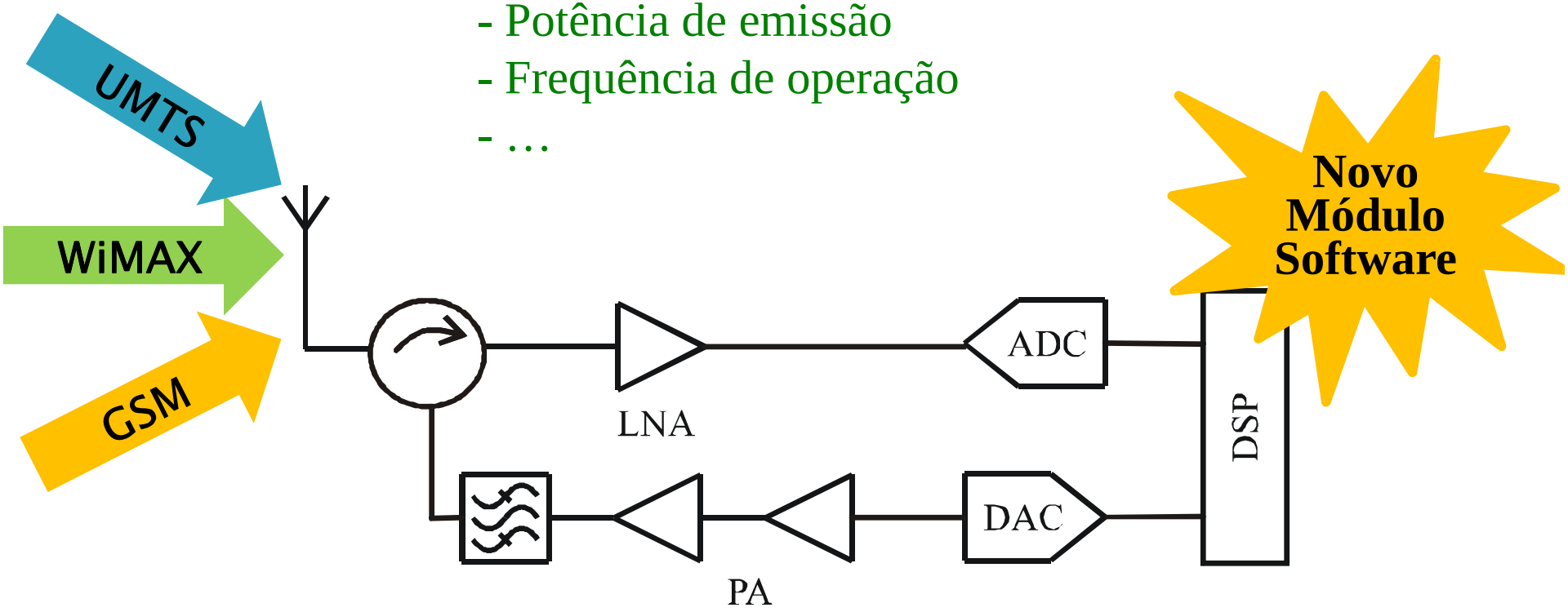
Rádio que seja reconfigurável por software e assim permitir a adaptação a vários cenários de comunicação



• **J. Mitola, "The software radio architecture",** ***IEEE Communications Magazine*****, vol. 33, nº 5, pp. 26–38, May 1995**

SDR Ideal (Conceito) – I

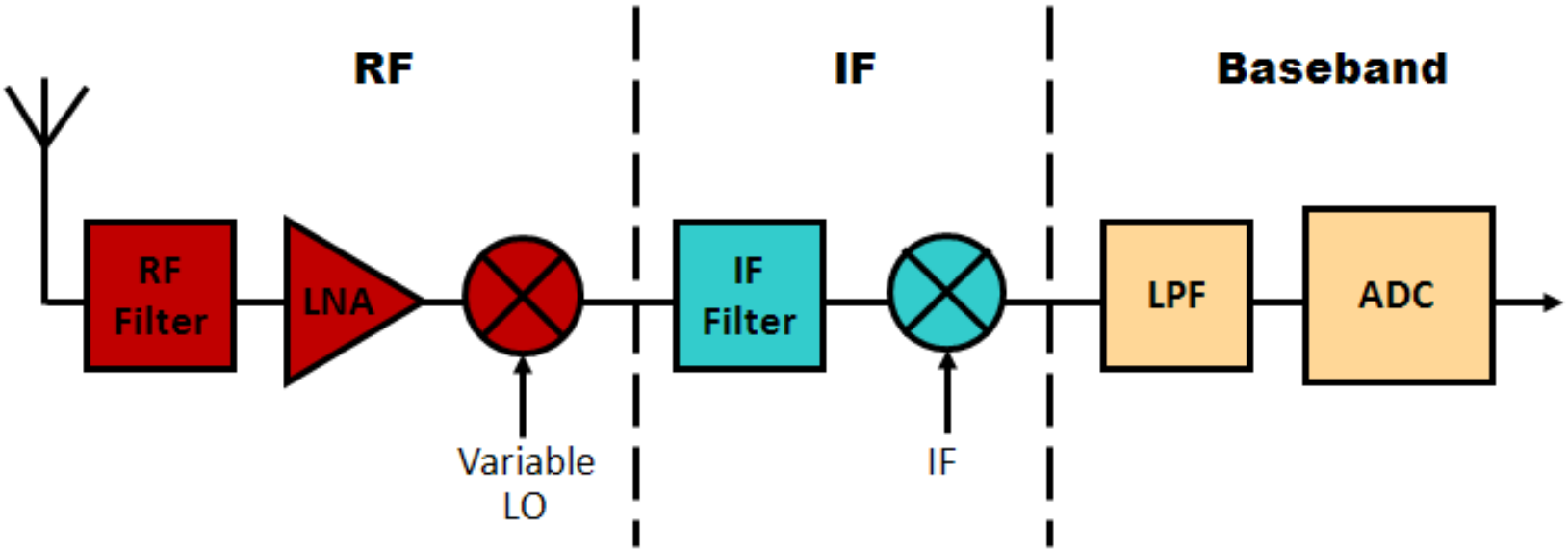
- Tipo de modulação
- Potência de emissão
- Frequência de operação
- …



• **J. Mitola, "The software radio architecture",** ***IEEE Communications Magazine*****, vol. 33, nº 5, pp. 26–38, May 1995**

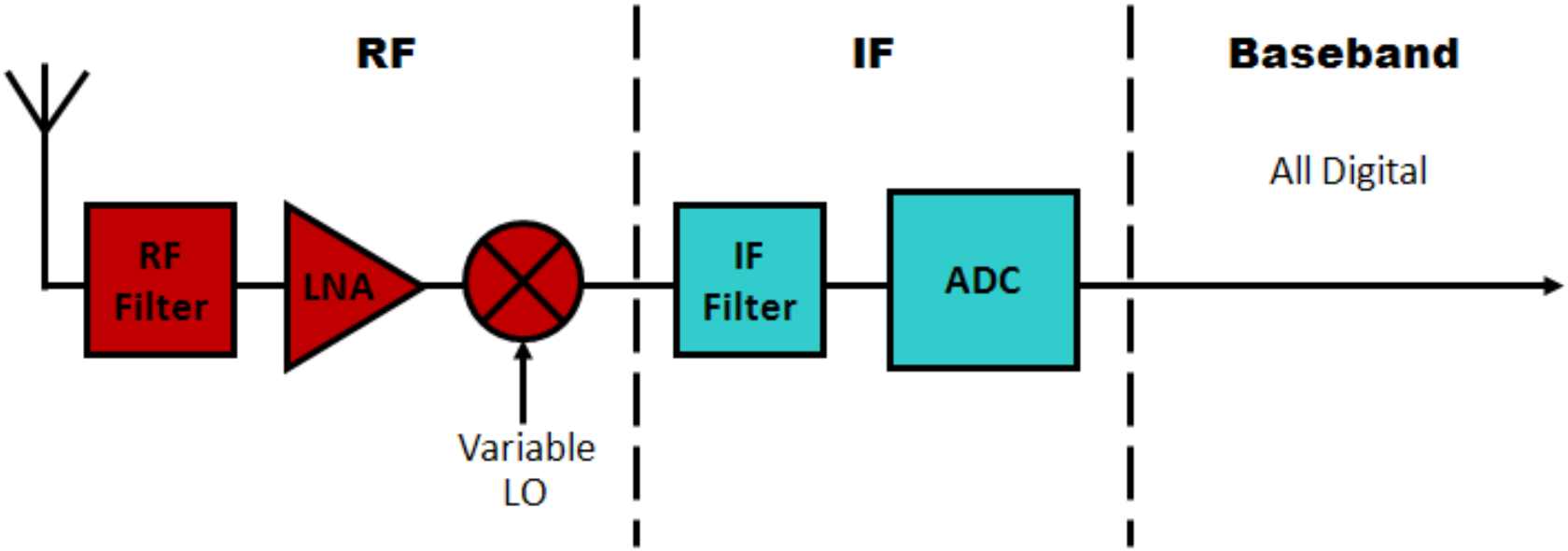
SDR Ideal (Conceito) – II

- Conversão do sinal analógico para digital feita a banda base
- Arquitectura adoptada na maioria dos receptores actuais
- Características de banda estreita logo não é adequada para ser usada em receptores de SDR



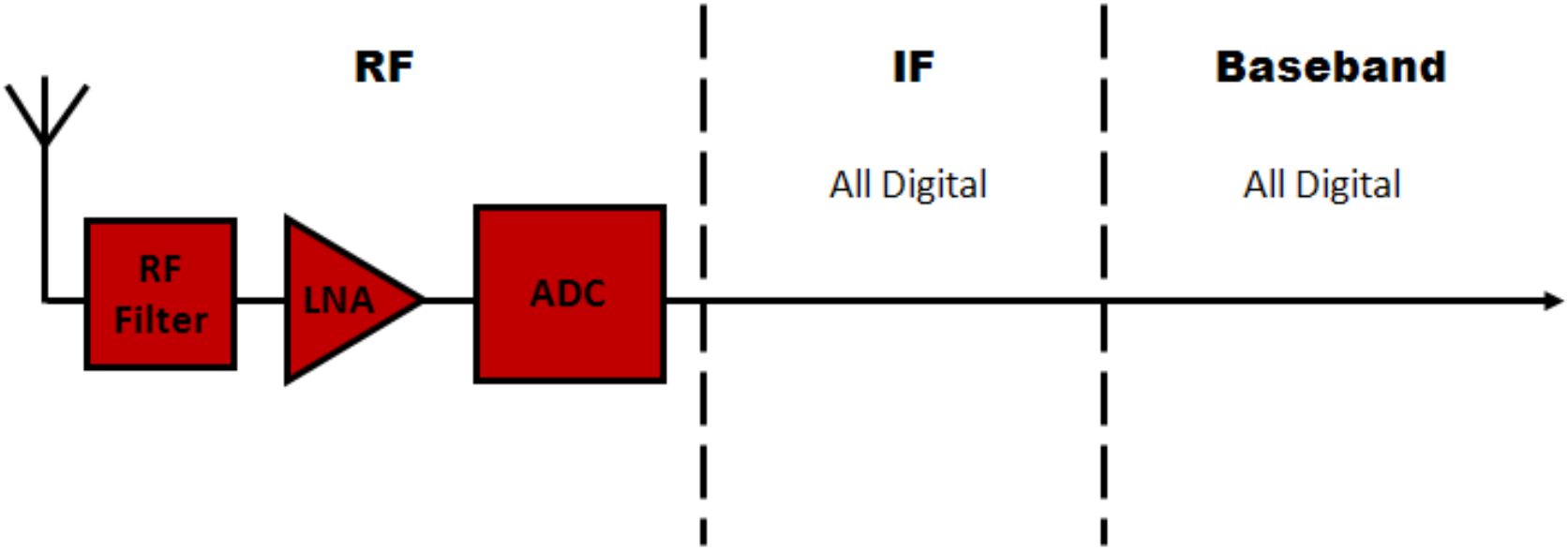
SDR Ideal (Conceito) – III

- ADC opera na frequência intermediária (IF)
- Pode ser projectada para operar numa maior largura de banda
- Configuração semelhante ao receptor de SDR ideal



SDR Ideal (Conceito) – IV

- Conversão do sinal analógico para digital em RF
- Corresponde à solução apresentada por J. Mitola
- Actualmente, muito difícil de realizar devido a algumas limitações dos componentes usados



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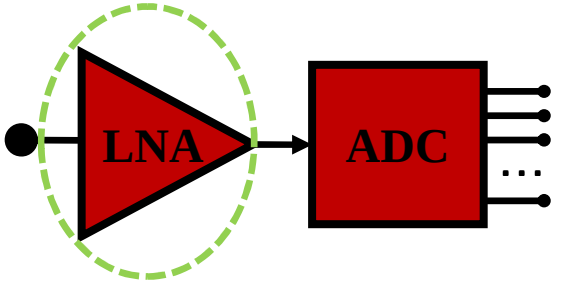
Distorção num Receptor de SDR – I

Amplificador de Baixo Ruído:



Sinal Fraco:

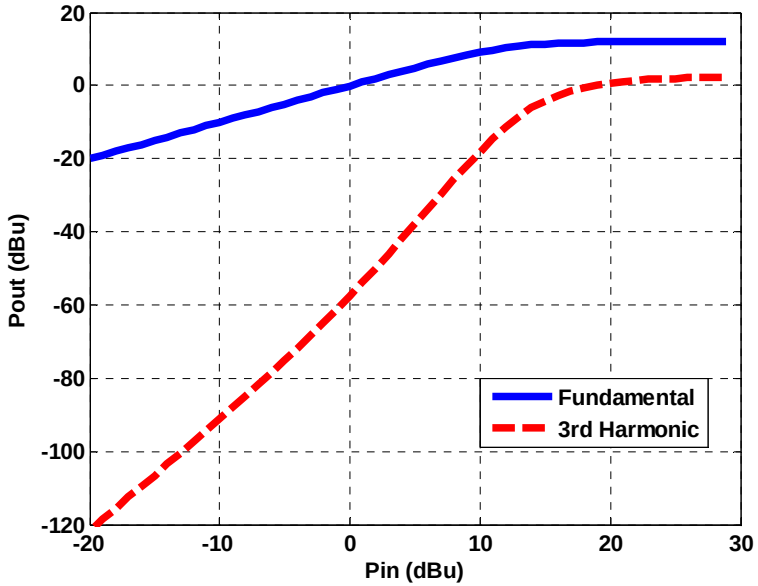
- Séries de Volterra $\longrightarrow$ $y_0(t) = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \cdots, \tau_n) * x(t-t_1) \cdots x(t-t_n) d\tau_1 \cdots d\tau_n$

- Polinómio de Taylor $\longrightarrow$ $y = a_1.x + a_2.x^2 + \cdots + a_n.x^n$

Sinal Forte:

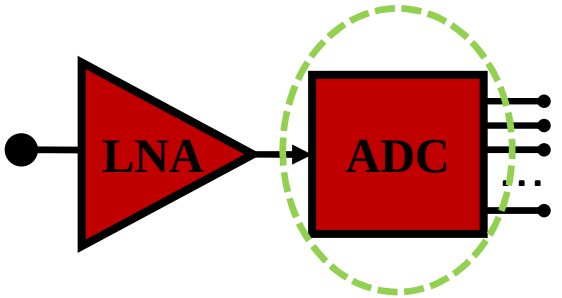
- Função Descritiva

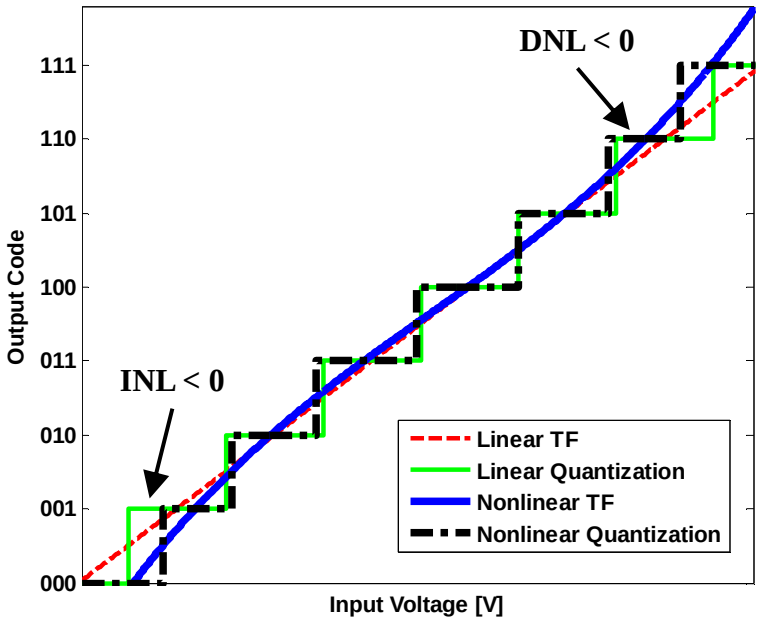
$y = \tanh(x)$



Distorção num Receptor de SDR – II

Conversor Analógico-Digital – F.T. não linear:



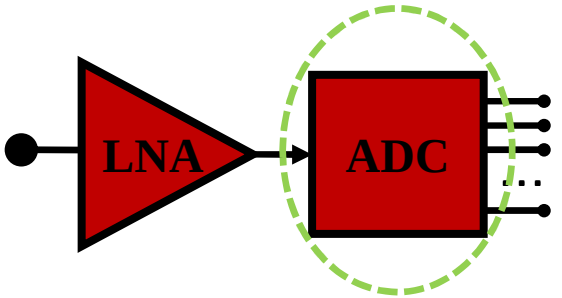


- Responsável por:
  - *Integral Nonlinearity* (INL)
  - *Differential Nonlinearity* (DNL)
  - Códigos (níveis) Perdidos

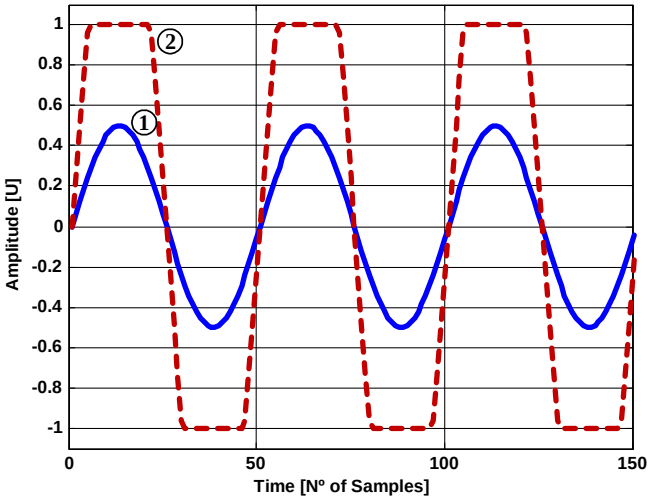
- Eficientemente modelada por uma função polinomial seguida de um *quantizer* ideal

Distorção num Receptor de SDR – II

Conversor Analógico-Digital - *Clipping*:

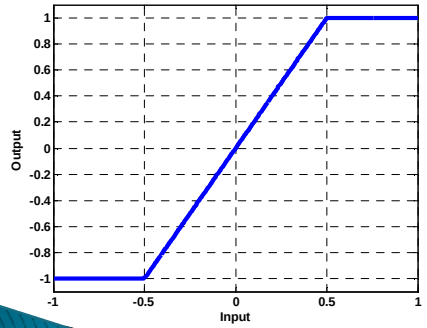


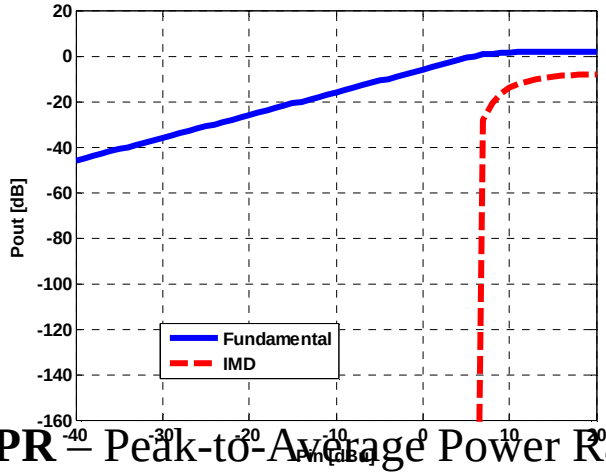
- Dependente da amplitude do sinal de entrada
- Importante nos sistemas de comunicação sem fios devido ao elevado PAPR dos sinais
- Num cenário real de SDR não sabemos a priori que sinais vamos receber (admitir *clipping*)



- Onda nº1: Sinal Fraco
- Onda nº2: Sinal Forte

Hard-Clipping

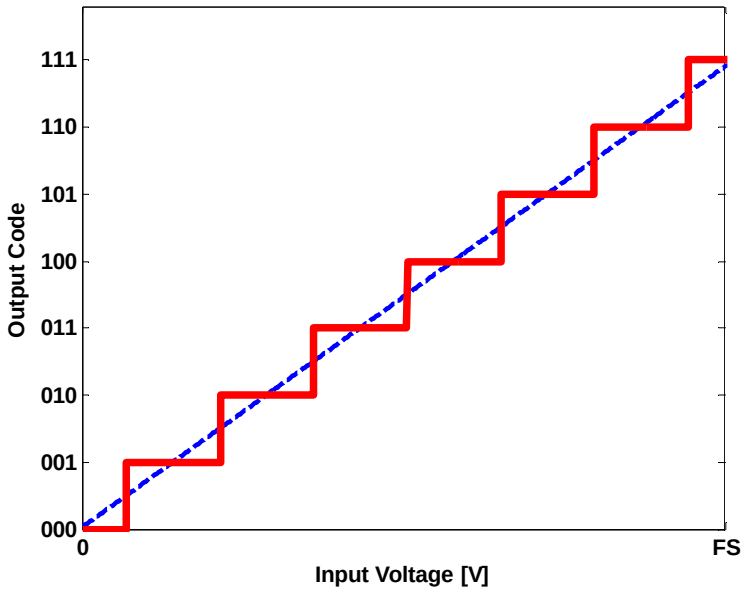


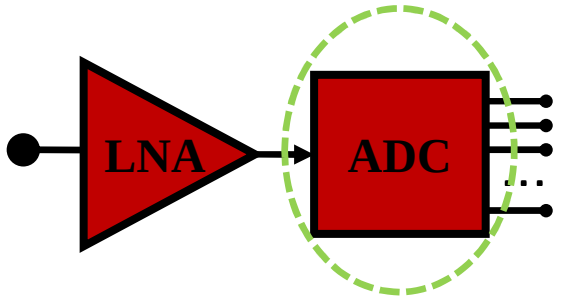


PAPR – Peak-to-Average Power Ratio

Distorção num Receptor de SDR – II

Conversor Analógico-Digital - Quantização:





- Transforma uma sinal analógico em níveis digitais
- Devido a este efeito o sinal de saída é composto por várias harmónicas (distorção)
- O erro de quantização diminui com o aumento do número de bits (N) da ADC

$$SNR_{dB} = 6.02 * N + 1.76$$

$$SNR_{dB} = 6.02 * N + 1.76 - \alpha + 10 * \log_{10}\left(\frac{f_s}{2 \times BW}\right)$$

PAPR **Ganho de Oversampling**

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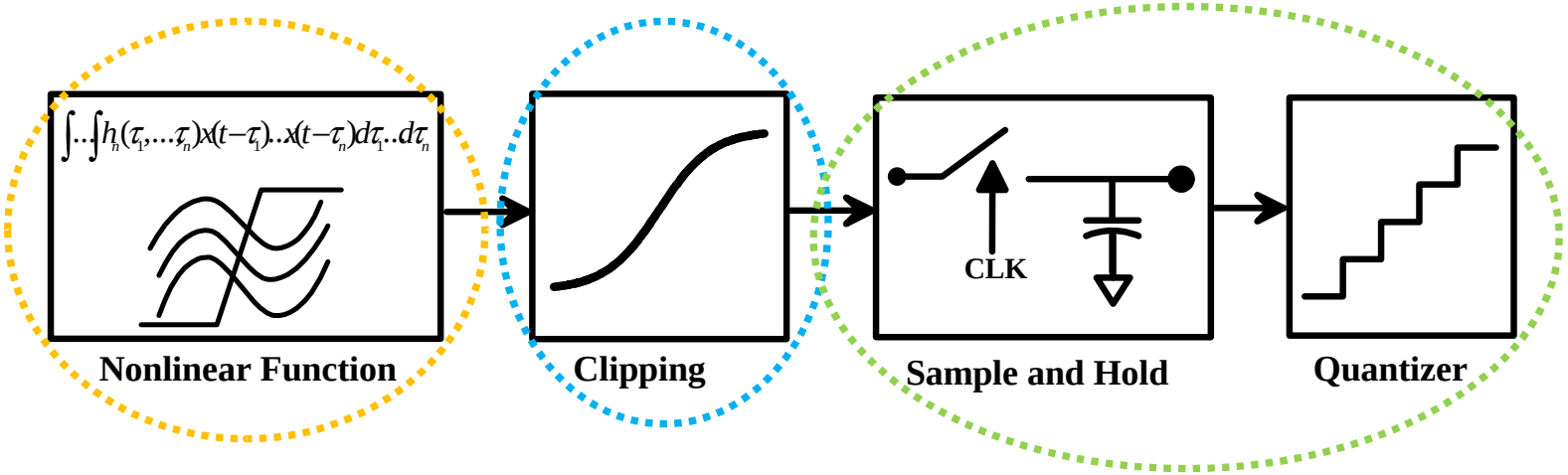
Modelo Comportamental do SDR – I

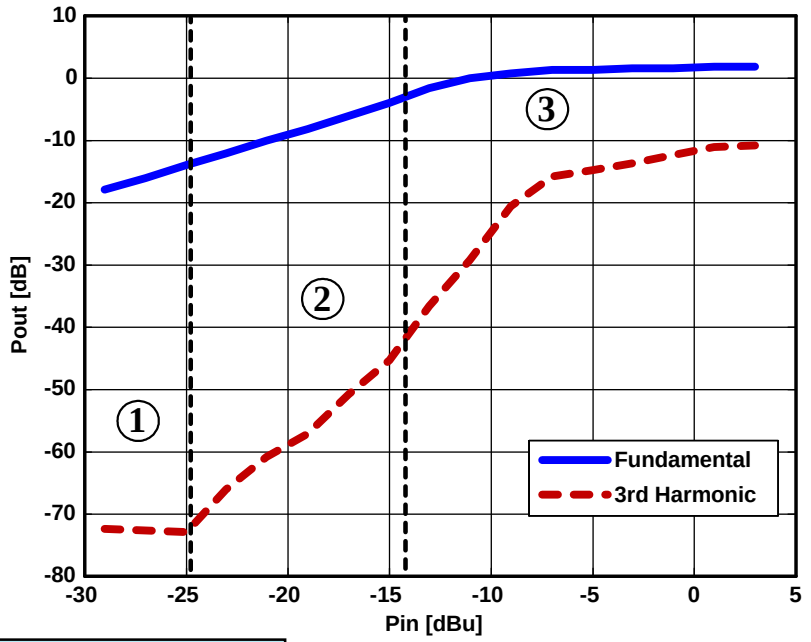


- Descreve as não linearidades nas F.T. do LNA e da ADC (sinal fraco)
  - Parâmetros do polinómio (Volterra) são extraídos a partir de medidas de sinal fraco
- Caracteriza a operação do LNA em sinal forte por uma tangente hiperbólica
  - Compressão da fundamental e da distorção definem os parâmetros da tangente hiperbólica
- Últimos blocos representam a amostragem e quantização feita pela ADC
  - *Full-scale* da ADC determina os valores limite do *quantizer*

Modelo Comportamental do SDR – II

- Nas medidas efectuadas usou-se um SDR constituído por:
  - LNA comercial (P_{1dB} = +9dBm)
  - $F_{central}$ na 3ª zona de Nyquist
  - FPB - evitar "*folding*" de outros sinais
  - ADC de 12 bits (LB_{in} = 750MHz)
  - Relógio (CLK) de 100MHz

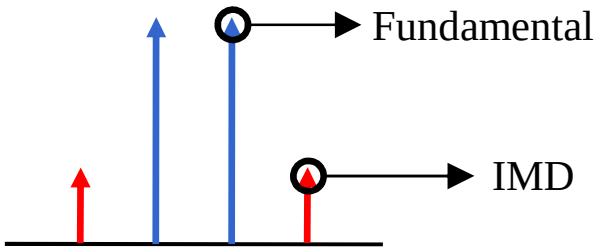
- Identificam-se 3 zonas diferentes:
  - A 1ª zona é eliminada da extracção de parâmetros devido ao nível de ruído
  - Da 2ª zona extraí-se o coeficiente de 3ª ordem
  - Da 3ª zona extraí-se o ponto de *clipping*



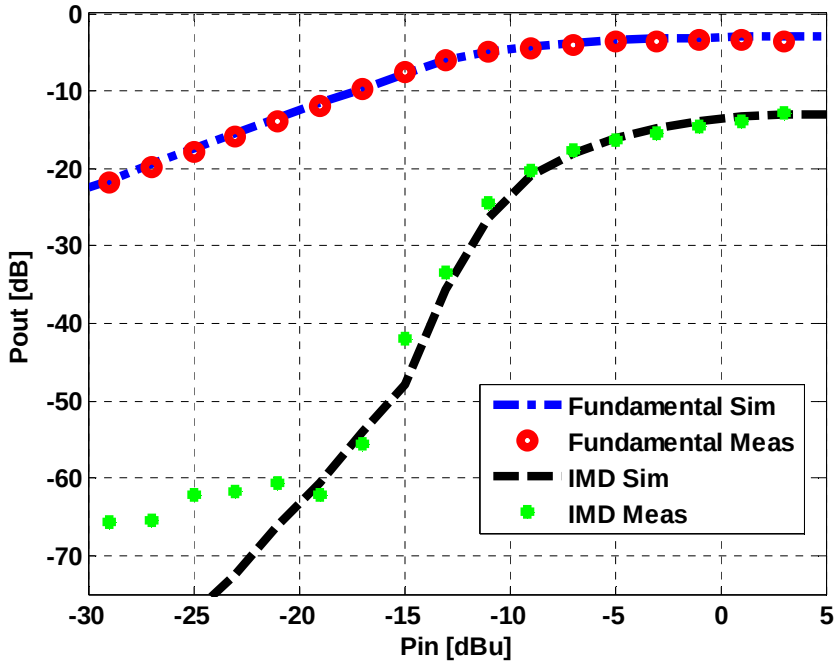
Parâmetros Extraídos

Modelo Comportamental do SDR – III

- Para verificar a validade do modelo aplicou-se um sinal de 2 tons



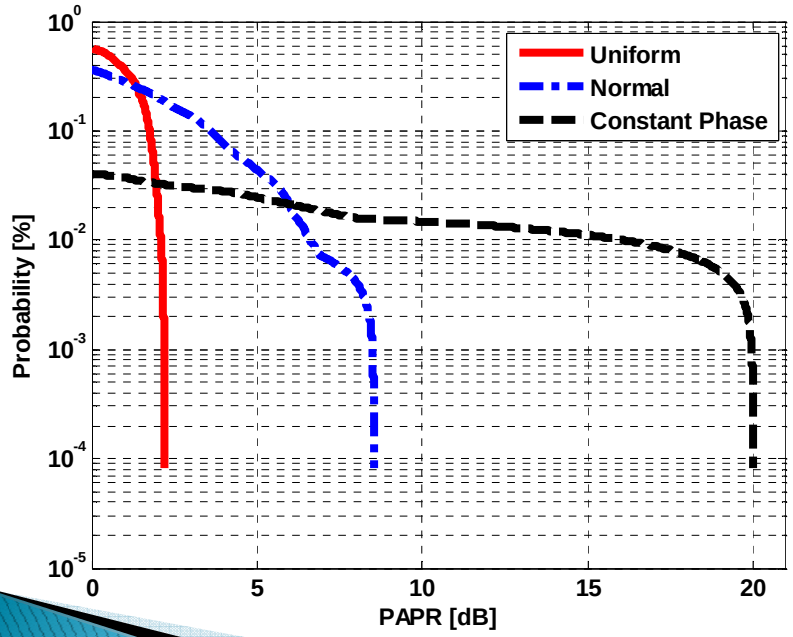
- Resultados muito semelhantes
- Variação do espaçamento entre tons não produziu diferenças
  - **Receptor usado é *"memoryless"***

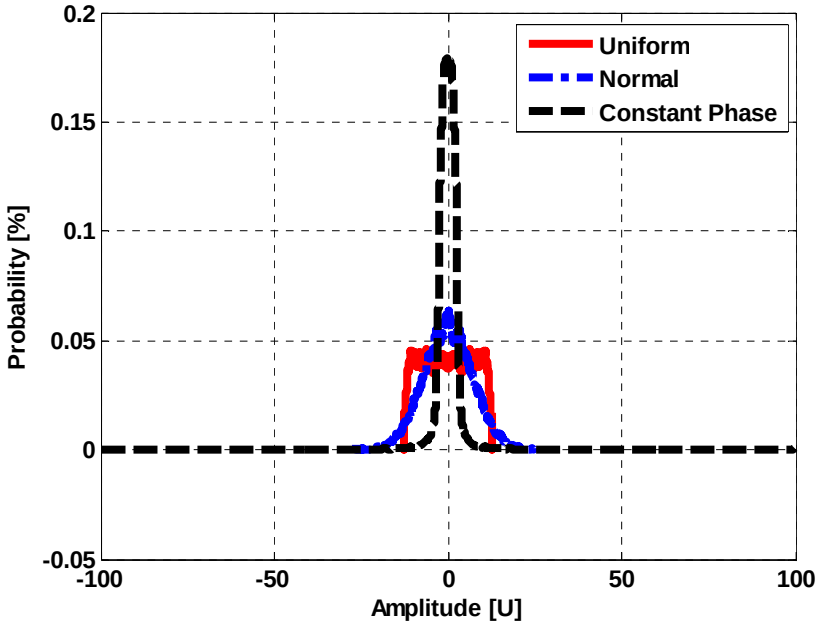


Modelo Comportamental do SDR – IV

- Desenho de Multisines (100 tons):

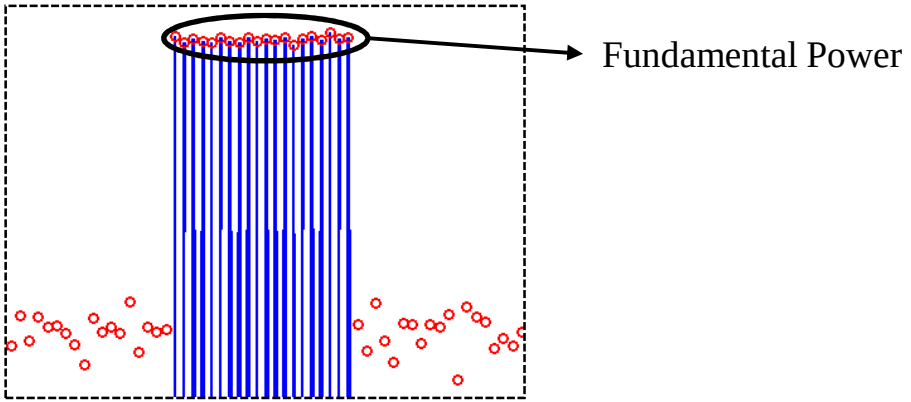
Signal Type	PAPR [dB]
Uniform	2.1266
Normal	8.5184
Constant Phase	20.0000



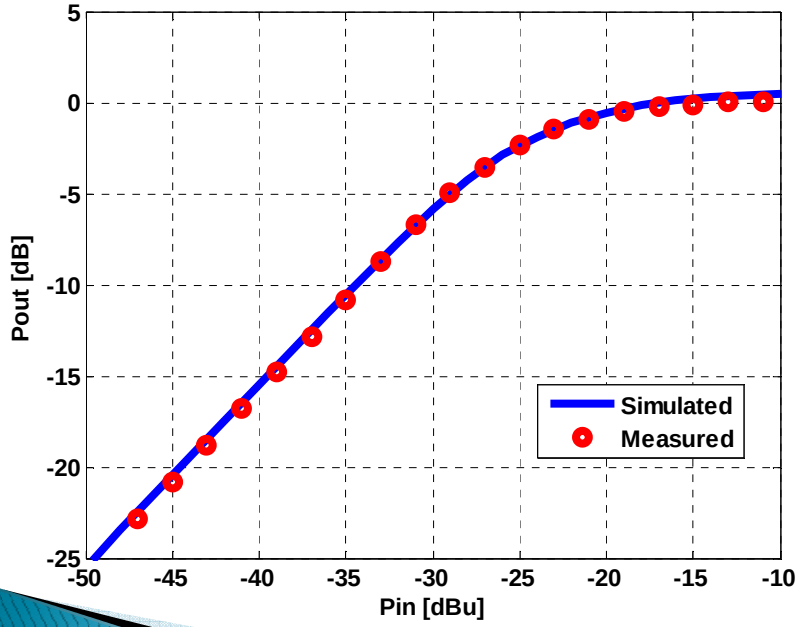


Modelo Comportamental do SDR – IV

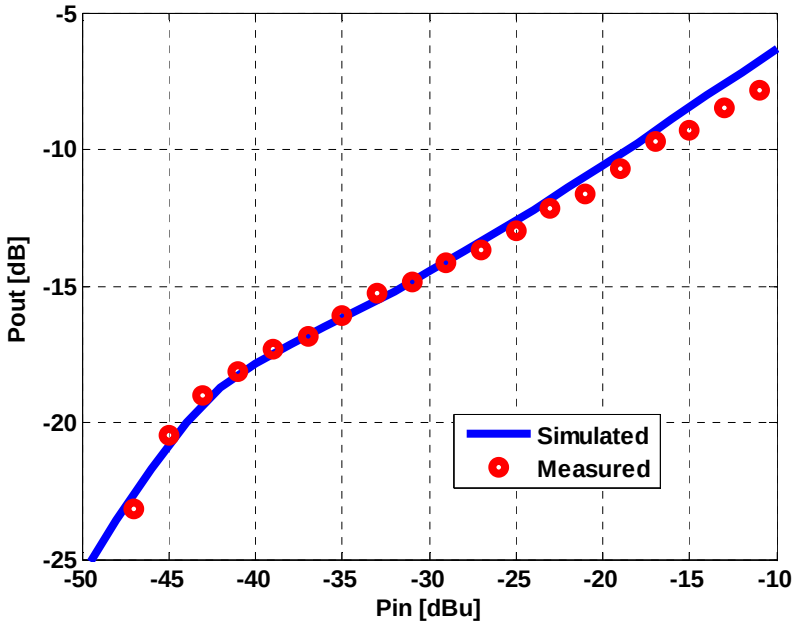
- Validação c/ Multisines:



Normal

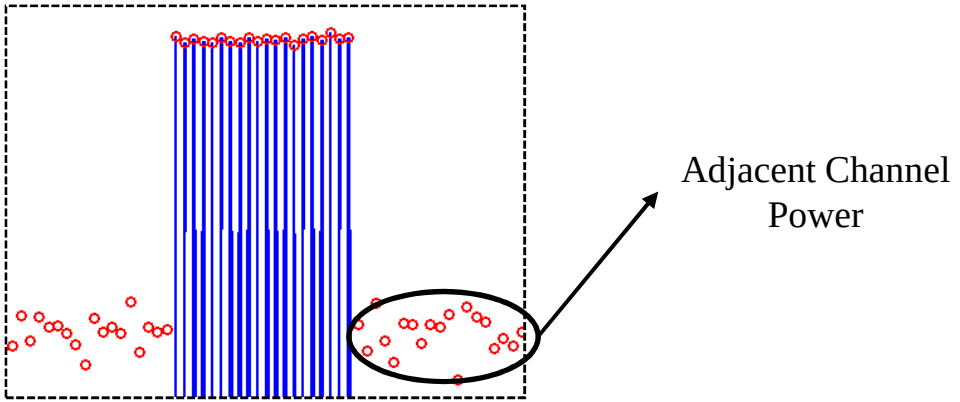


Constant Phase

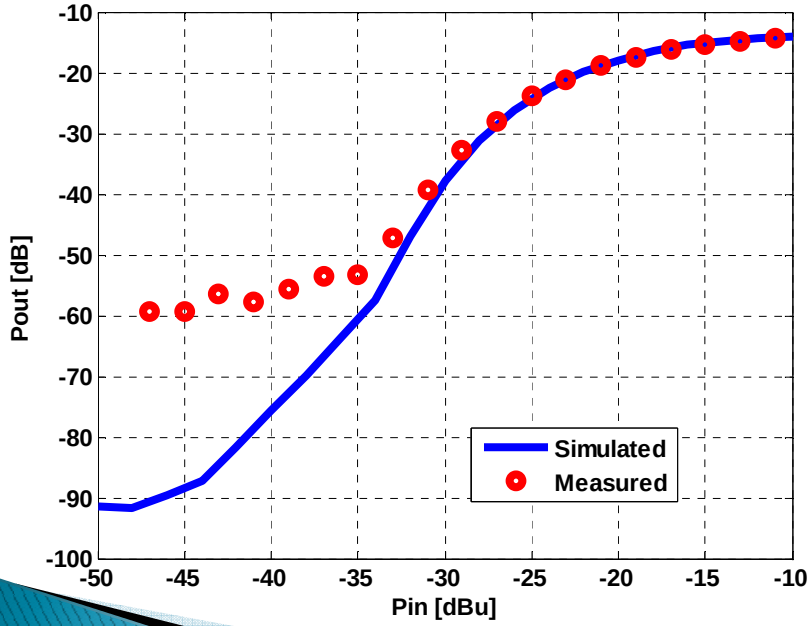


Modelo Comportamental do SDR – IV

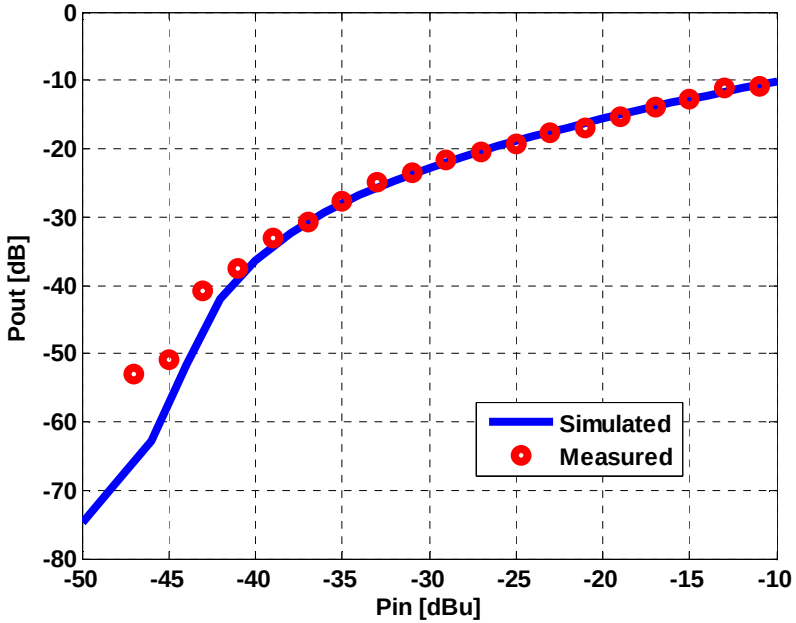
- Validação c/ Multisines:



Normal



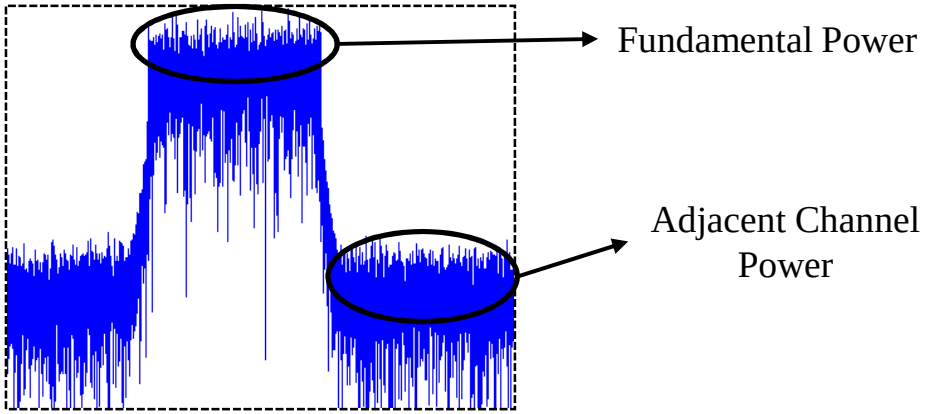
Constant Phase

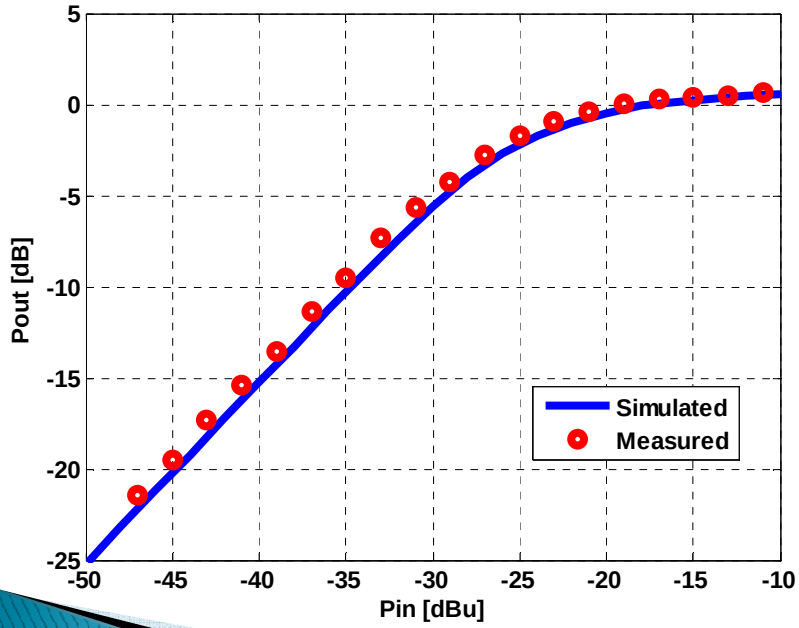


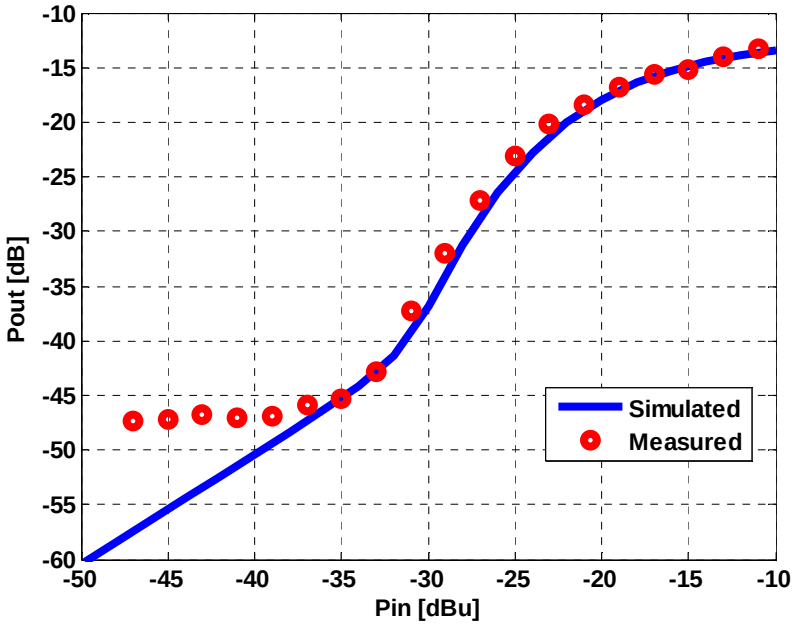
Modelo Comportamental do SDR – V

- Validação c/ WiMax:

- 64-QAM (¾)
- LB = 3 MHz
- PAPR = 9.5266 dB







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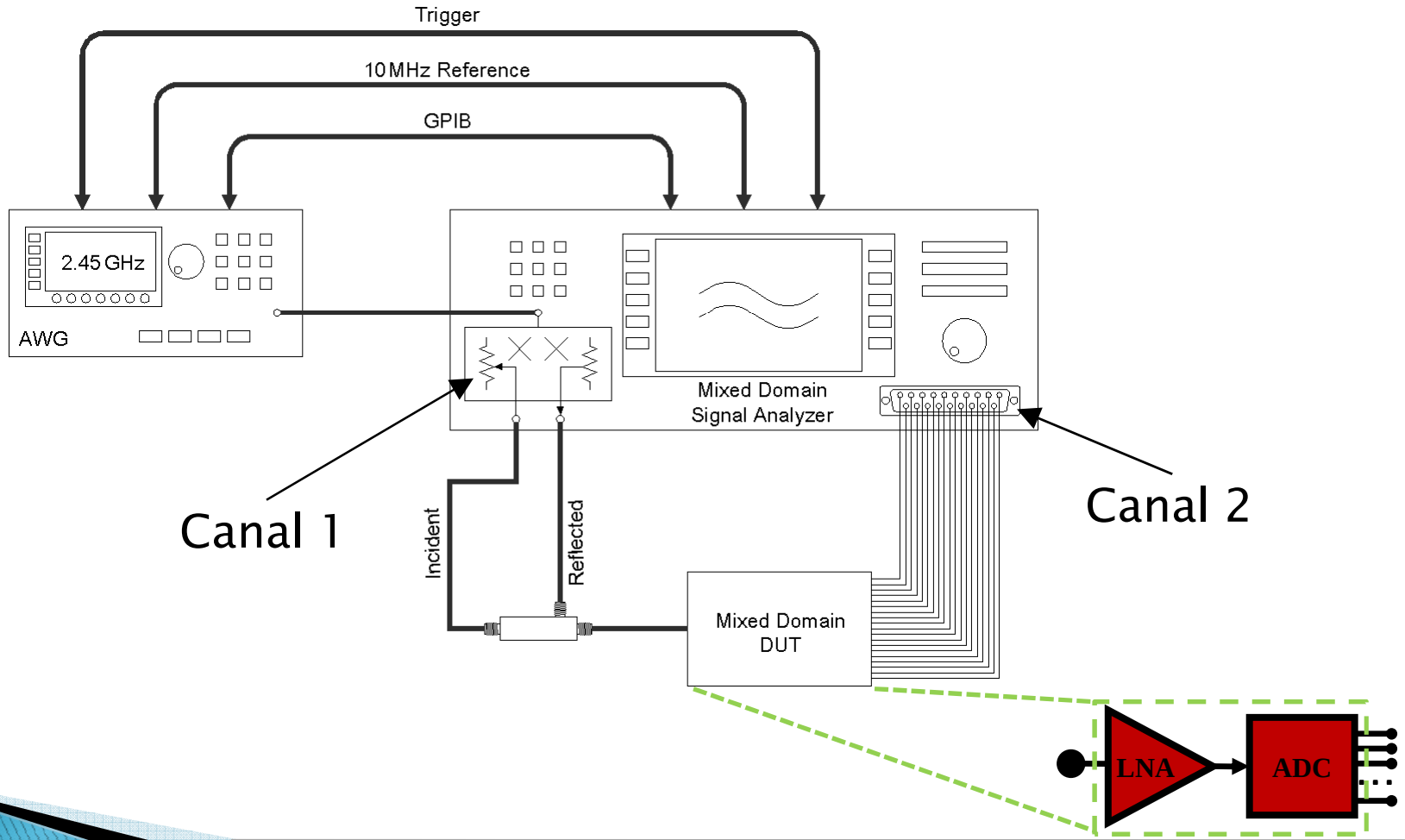
Instrumentação Proposta – I

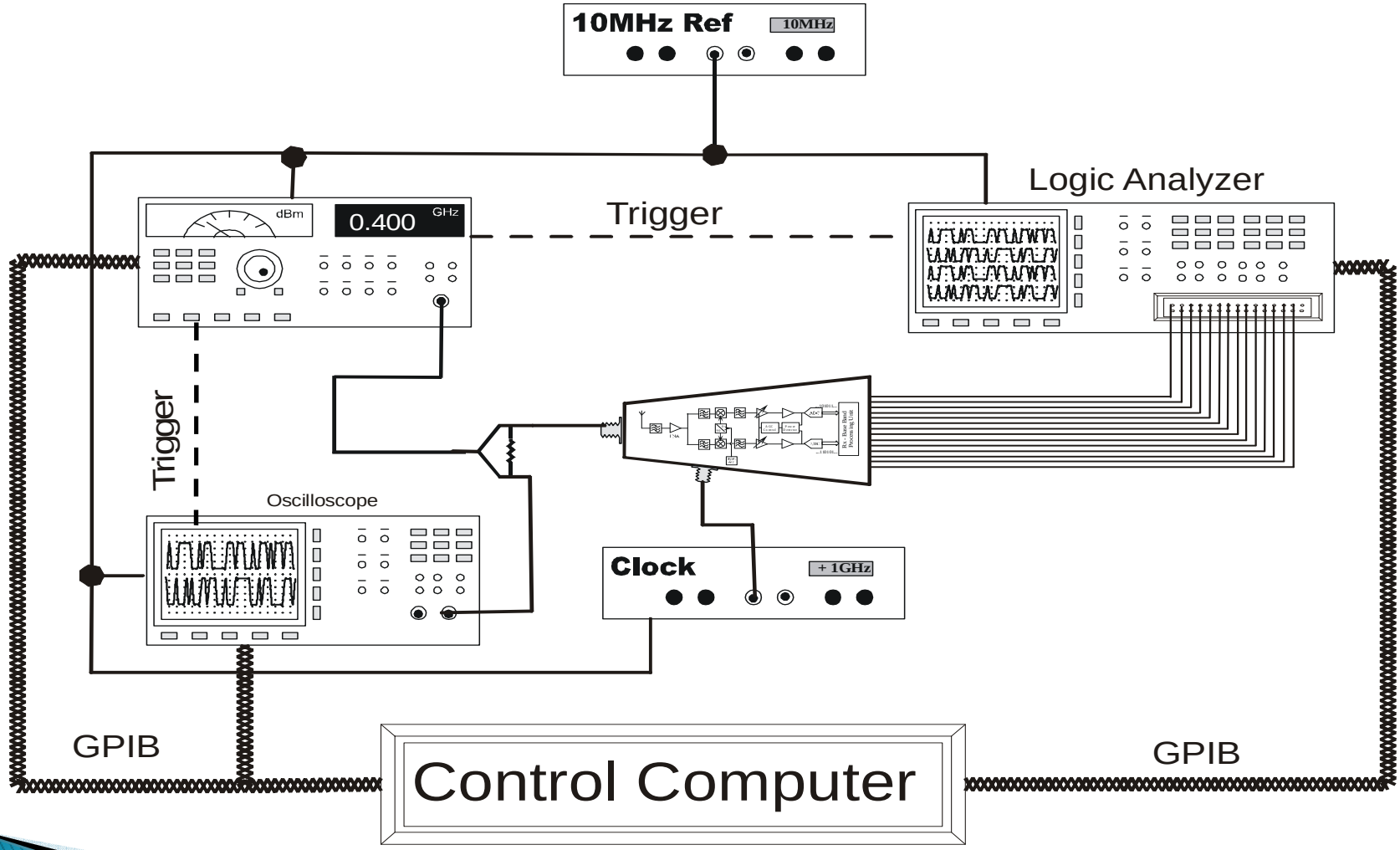
Canal Analógico (1) → **Analisador de Redes / Osciloscópio**

Canal Digital (2) → **Analisador Lógico**



Instrumentação Proposta – II

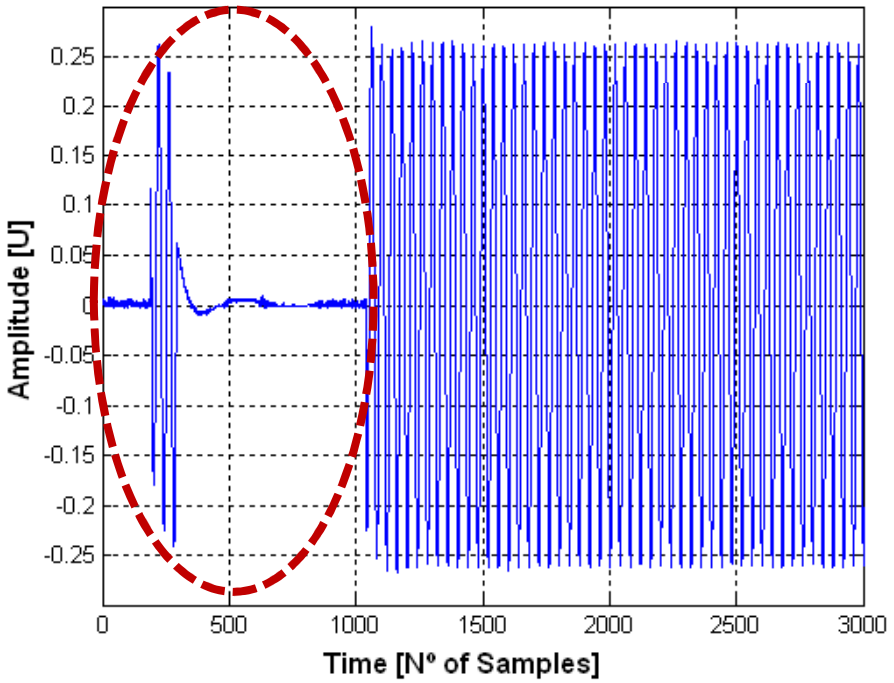
Implementação Laboratorial:



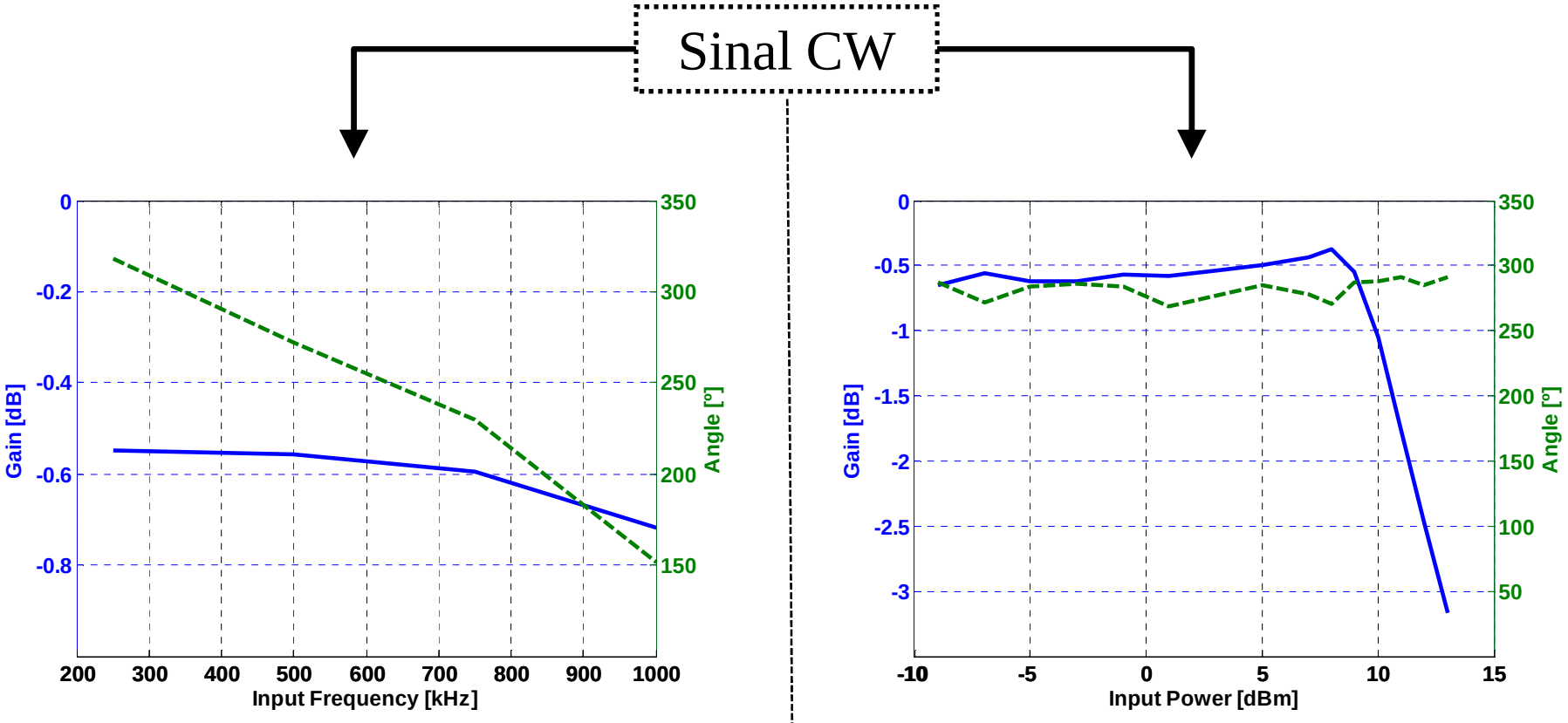
Instrumentação Proposta – III

Solução p/ Sincronismo (*Trigger*):

- Sinais de trigger sofrem de *time drift*
- Erros devido a medidas não sincronizadas, etc.
- **Solução:** Usar um sinal de *trigger* no sinal de entrada



Instrumentação Proposta – IV



- Ganho do DUT é praticamente constante
- Variação de fase decresce linearmente

- Representa as curvas AM/AM (azul) e AM/PM (verde) do DUT

Sumário

- Software Defined Radio Ideal (Conceito)
- Distorção num Receptor de SDR
- Modelo Comportamental do SDR
  - Resultados Obtidos
- Instrumentação Proposta
- Conclusões

Conclusões

- Apresentou-se um estudo detalhado sobre os mecanismos de distorção presentes num receptor de SDR
- Propôs-se um modelo comportamental para caracterização da distorção num receptor de SDR
- Obteve-se grande concordância entre as simulações (modelo) e as medidas usando o receptor de SDR
- Apresentou-se uma nova instrumentação para caracterização de receptores e/ou transmissores de SDR com base em simples equipamento de laboratório

Publicações

- ✓ Pedro Cruz e Nuno B. Carvalho, "PAPR Evaluation in Multi-Mode SDR Transceivers", *European Microwave Conference*, Amesterdão, Holanda, Outubro 2008
- ✓ Pedro Cruz, Nuno B. Carvalho, Kate A. Remley e Kevin G. Gard, "Mixed Analog-Digital Instrumentation for Software Defined Radio Characterization", *IEEE MTT-S International Microwave Symposium*, Atlanta, GA, United States, Junho 2008
- ✓ Pedro Cruz, Nuno B. Carvalho e Kate A. Remley, "Evaluation of Nonlinear Distortion in ADCs Using Multisines", *IEEE MTT-S International Microwave Symposium*, Atlanta, GA, United States, Junho 2008

Obrigado pela sua atenção!